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Flaircomm Microelectronics, Inc.

FLC-CBM383/6/7
FLC-CBM283/6/7
Datasheet

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Release Record

Version	Release Date	Comments
1.0	May 27, 2013	First Release
1.1	May 30, 2013	Optimize Pin Definition. Add GLONASS Frequency Band. Small modification.
1.2	June 19, 2013	Small Modification about Introduction.
1.3	June 24, 2013	Modify Pin Definitions: IRQ_WL polarity, SDIO Pull requirements, etc.; Modify Figure 3: WLAN Power Up Sequence; Add comment on max operating conditions (VBAT) and sleep currents updated.
1.4	August 8, 2013	Update Table 2. (Add Standby Current & Weight)
1.5	Nov. 26, 2013	Modify package information in Part 9: Mechanical Characteristic.
1.6	Feb. 11, 2014	Improve Section 3.2: Pin Definition.
1.7	May 12, 2014	Update Pin Definition of some pinouts. Update some performance parameters of the modules.
1.8	Mar. 16, 2015	Update figure 21. (Modify tolerance)
1.9	Jan. 18, 2016	Add “WL/BT Dual Antenna” modules. Remove secondary clock. Modify power-up and shutdown states. Add ESD and reliability test.
2.0	Nov. 23, 2016	Modify description about pin55 (table 4). Modify mechanical characteristic (figure 20).

CONTENTS

TABLES AND FIGURES

1. Introduction

This datasheet describes the FLC-CBM38x and FLC-CBM28x (where x=3, 6, 7) series of multi-function wireless connectivity modules. These modules are based on TI WL8Q and WL8 chipset. They are highly integrated modules that incorporate WLAN, BT, BLE and GNSS in a single package. Any module in this series shares the same 56 pin 20mmx21mm QFN package. The package sharing provides a universal platform to meet all wireless connectivity needs in vehicle infotainment device. This device is ideal for addressing all wireless multimedia options within a modern car be it the head unit infotainment console or the rear seat display unit. This series modules offer two different product grades (A – Automotive, I – Industrial). Any a grade module in this series is based on TI WL8Q chipset. Any I grade module in this series is based on TI WL8 chipset.

- High quality audio based Bluetooth hands-free calling and music
- Multiple Bluetooth connections active simultaneously
- High Definition video sharing between personal portable device and in car infotainment system
- Screen mirroring over Wifi Miracast TM
- GPS and GLONASS based accurate position information

1.1 Module Functional Blocks

Product Name	WLAN 2.4GHz	WLAN 5GHz	WLAN 2.4G MIMO	BT, BLE	WL/BT Shared Antenna	WL/BT Dual Antenna	GNSS
CBM383AQ2A	√	√	√	√	√		√
CBM283AQ2A	√	√	√	√	√		
CBM386AQ2A	√	√		√	√		√
CBM286AQ2A	√	√		√	√		
CBM387AQ2A	√			√	√		√
CBM287AQ2A	√			√	√		
CBM383IQ2A	√	√	√	√	√		√
CBM283IQ2A	√	√	√	√	√		
CBM386IQ2A	√	√		√	√		√
CBM286IQ2A	√	√		√	√		

CBM387IQ2A	√			√	√		√
CBM287IQ2A	√			√	√		
CBM383AQ2B	√	√	√	√		√	√
CBM283AQ2B	√	√	√	√		√	
CBM386AQ2B	√	√		√		√	√
CBM286AQ2B	√	√		√		√	
CBM387AQ2B	√			√		√	√
CBM287AQ2B	√			√		√	
CBM283IQ2B	√	√	√	√		√	
CBM286IQ2B	√	√		√		√	
CBM287IQ2B	√			√		√	

Table 1: Module Functional Blocks

1.2 Block Diagram

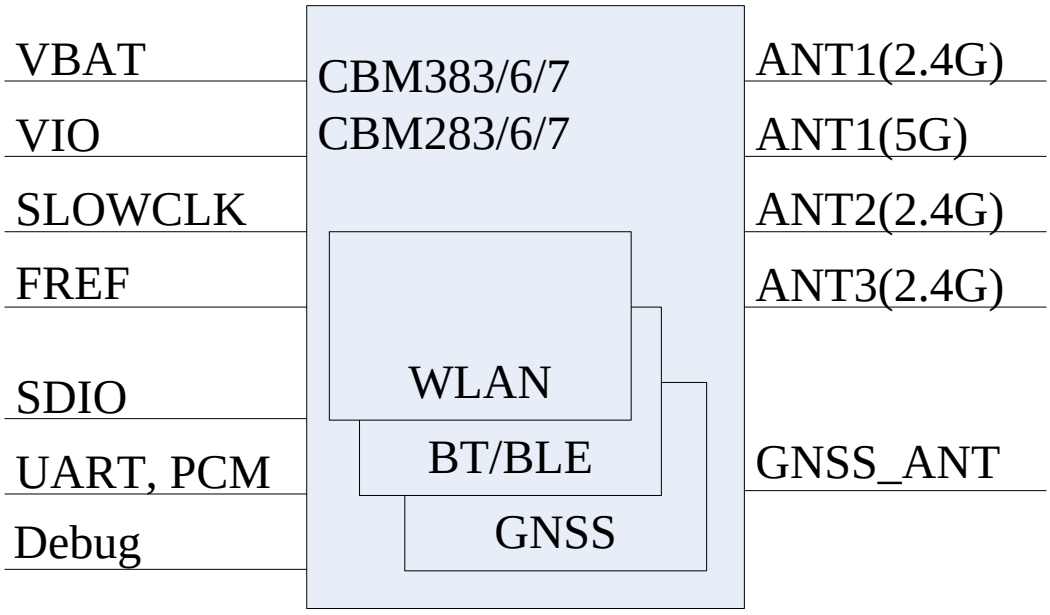

Figure 1: Block Diagram

1.3 Features

- WLAN, BT, BLE, GNSS on a single package provides a unique scalable platform catering to all connectivity needs in vehicle infotainment

- Provides efficient direct connection to battery by employing several integrated switched mode power supplies (DC/DC).
- Shared HCI transport for BT/BLE/GNSS over UART and SDIO for WLAN.
- Downloadable patches and firmware enable new features to be added for all functional blocks.
- Temperature detection and compensation mechanism ensures minimal variation in RF performance over the entire temperature range. (-40°C to 85°C)
- BT 4.0, BLE and all audio processing features work in parallel and include full coexistence with WLAN

1.3.1 Bluetooth Features

- Supports Bluetooth 4.0 BLE
- Includes concurrent operation and built-in coexisting and prioritization handling of BT, BLE audio processing and WLAN
- Dedicated Audio processor supporting on chip SBC encoding + A2DP:
  - Assisted A2DP (A3DP) support - SBC encoding implemented internally - per BT specification
  - Assisted WB-Speech (AWBS) support - modified SBC codec implemented internally

1.3.2 BLE Features

- Fully compliant with BT4.0 BLE dual mode standard
- Support for all roles and role-combinations, mandatory as well as optional
- BLE solution optimized for the fitness, health and proximity use-cases
- Supports multiple connections (up to 10)
- Multiple sniff instances are tightly coupled to achieve minimum power consumption
- Independent buffering for LE allows having large number of multiple connections without affecting BDR/EDR performance

1.3.3 WLAN Features

- Integrated 2.4 & 5 GHz PAs, switches and filters for complete WLAN solution
- WLAN MAC baseband processor and RF transceiver - IEEE802.11a/b/g/n compliant
- WLAN 11n 40MHz (SISO) and 11n 20MHz (SISO and MIMO)
- Baseband Processor

- IEEE Std 802.11a/b/g data rates and IEEE Std 802.11n data rates with 20 or 40 MHz SISO and 20 MHz MIMO

- Fully calibrated system. No production calibration required.
- Medium Access Controller (MAC)
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys
  - Supports requirements for Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [includes hardware-accelerated Advanced Encryption Standard (AES)]
  - Designed to work with IEEE Std 802.1x
- IEEE Std 802.11d,e,h,i,k,r PICS compliant
- New advanced co-existence scheme with BT/BLE
- 2.4/5.0 GHz Radio
  - Supports: IEEE Std 802.11a, 802.11b, 802.11g and 802.11n
- Supports 4 bit SDIO host interface, including high speed mode

1.3.4 GNSS Features

- On-chip position engine
- Simultaneous processing of GPS, GLONASS, QZSS and SBAS satellite systems
- Support for up to 36 acquisition channels
- 16 dedicated high resolution tracking channels for GPS, SBAS and QZSS satellites
- 9 dedicated high resolution tracking channels for GLONASS
- SBAS support
- Increased flexibility in receiver core for coexistence (frequency avoidance, improved PA blanking, etc.)
- Operation through Bluetooth host interfaces (shared transport)

2. General Specification

Bluetooth	
Standard	Bluetooth 4.0 (Dual Mode)
Profiles	A2DP, WBS, etc. Detailed profiles depend on upper PS/Profile sets running on host.
Frequency Band	2.402G ~ 2.480G
RF Input Impedance	50 ohms
Interfaces	UART, PIO, PCM/I^2S
WLAN	
Frequency Band	2.4/5.0 GHz
RF Input Impedance	50 ohms
Interfaces	SDIO
GPS and GNSS	
GPS Frequency Band	1575.42 MHz
GLONASS Frequency Band	1602 MHz
RF Input Impedance	50 ohms
Interfaces	UART
Power	
Supply Voltage	2.9 ~ 4.8V DC
Working Current	BT: 33mA @ EDR full throughput
	WLAN: TBD
Standby Current	<200uA
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Certifications	BQB
Environmental	RoHS Compliant
Dimension and Weight	
Dimension	21mm(L)*20mm(W)*2.8mm(H)
Weight	2.10~2.25g

Table 2: General Specification

3. Pin Definition

3.1 Pin Configuration

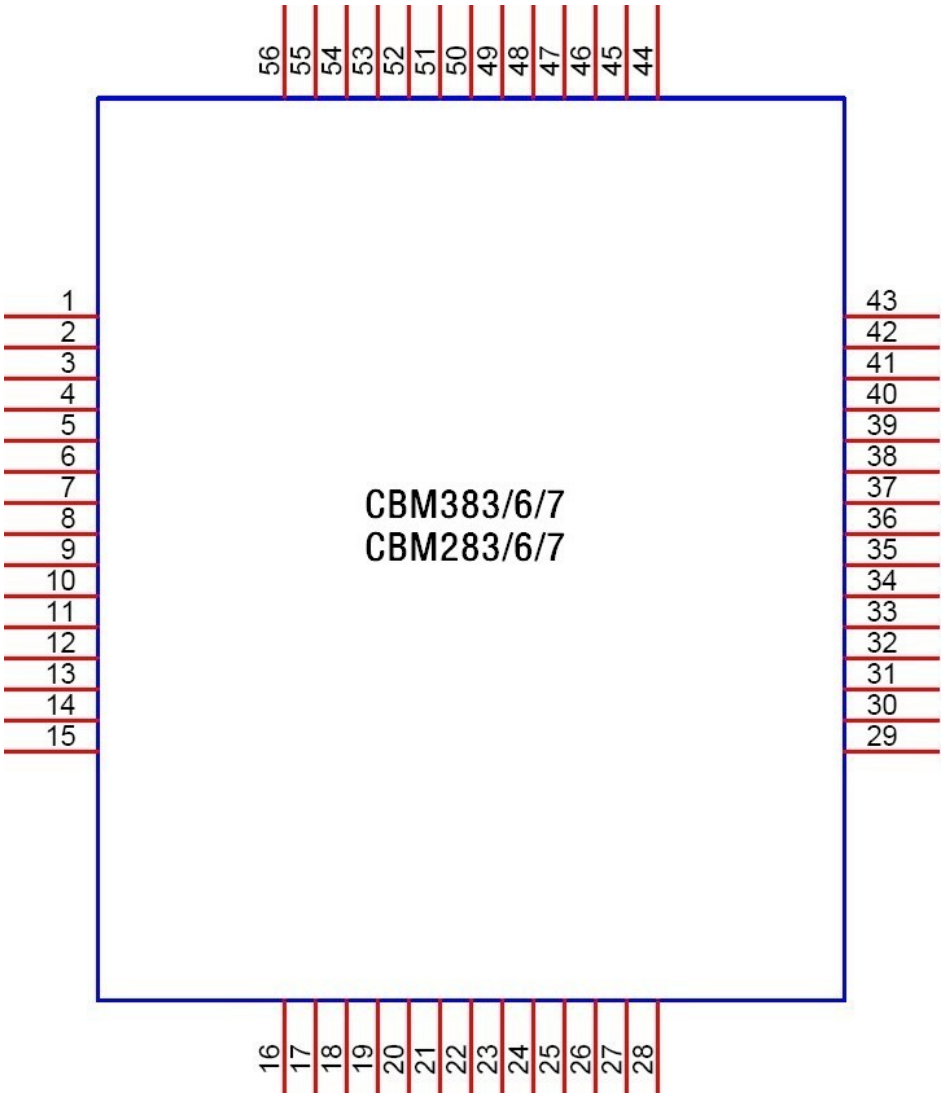

Figure 2: Pin Configuration

Pin	CBM383	CBM283	CBM386	CBM286	CBM387	CBM287
1	ANT1(5G)	ANT1(5G)	ANT1(5G)	ANT1(5G)	NC	NC
2	GND	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND
4	ANT1(2.4G)	ANT1(2.4G)	ANT1(2.4G)	ANT1(2.4G)	ANT1(2.4G)	ANT1(2.4G)
5	GND	GND	GND	GND	GND	GND
6	WL_EN	WL_EN	WL_EN	WL_EN	WL_EN	WL_EN
7	BT_EN	BT_EN	BT_EN	BT_EN	BT_EN	BT_EN
8	WL_RS232_RX	WL_RS232_RX	WL_RS232_RX	WL_RS232_RX	WL_RS232_RX	WL_RS232_RX
9	GNSS_PA_EN	NC	GNSS_PA_EN	NC	GNSS_PA_EN	NC
10	GPS_PPS_OUT	NC	GPS_PPS_OUT	NC	GPS_PPS_OUT	NC
11	UART_DBG_WL	UART_DBG_WL	UART_DBG_WL	UART_DBG_WL	UART_DBG_WL	UART_DBG_WL
12	IRQ_WL	IRQ_WL	IRQ_WL	IRQ_WL	IRQ_WL	IRQ_WL
13	VBAT	VBAT	VBAT	VBAT	VBAT	VBAT
14	NC	NC	NC	NC	NC	NC
15	RTC_CLK	RTC_CLK	RTC_CLK	RTC_CLK	RTC_CLK	RTC_CLK
16	SDIO_D3_WL	SDIO_D3_WL	SDIO_D3_WL	SDIO_D3_WL	SDIO_D3_WL	SDIO_D3_WL
17	SDIO_D0_WL	SDIO_D0_WL	SDIO_D0_WL	SDIO_D0_WL	SDIO_D0_WL	SDIO_D0_WL
18	SDIO_D2_WL	SDIO_D2_WL	SDIO_D2_WL	SDIO_D2_WL	SDIO_D2_WL	SDIO_D2_WL
19	SDIO_D1_WL	SDIO_D1_WL	SDIO_D1_WL	SDIO_D1_WL	SDIO_D1_WL	SDIO_D1_WL
20	SDIO_CMD_WL	SDIO_CMD_WL	SDIO_CMD_WL	SDIO_CMD_WL	SDIO_CMD_WL	SDIO_CMD_WL
21	SDIO_CLK_WL	SDIO_CLK_WL	SDIO_CLK_WL	SDIO_CLK_WL	SDIO_CLK_WL	SDIO_CLK_WL
22	VIO	VIO	VIO	VIO	VIO	VIO
23	NC	NC	NC	NC	NC	NC
24	NC	NC	NC	NC	NC	NC
25	NC	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC	NC
29	EXT_LNA_EN_GNSS	EXT_LNA_EN_GNSS	EXT_LNA_EN_GNSS	EXT_LNA_EN_GNSS	EXT_LNA_EN_GNSS	EXT_LNA_EN_GNSS
30	GND	GND	GND	GND	GND	GND
31	GNSS_ANT	NC	GNSS_ANT	NC	GNSS_ANT	NC
32	GND	GND	GND	GND	GND	GND
33	NC	NC	NC	NC	NC	NC
34	UART_DBG_BT	UART_DBG_BT	UART_DBG_BT	UART_DBG_BT	UART_DBG_BT	UART_DBG_BT
35	TIMESTAMP	NC	TIMESTAMP	NC	TIMESTAMP	NC
36	383A:IRQ_GNSS/383I:NC	NC	386A:IRQ_GNSS/386I:NC	NC	387A:IRQ_GNSS/387I:NC	NC
37	PERIPH_I2C_SDA_GNSS	NC	PERIPH_I2C_SDA_GNSS	NC	PERIPH_I2C_SDA_GNSS	NC
38	PERIPH_I2C_SCL_GNSS	NC	PERIPH_I2C_SCL_GNSS	NC	PERIPH_I2C_SCL_GNSS	NC
39	HCI_CTS_BT	HCI_CTS_BT	HCI_CTS_BT	HCI_CTS_BT	HCI_CTS_BT	HCI_CTS_BT
40	HCI_RTS_BT	HCI_RTS_BT	HCI_RTS_BT	HCI_RTS_BT	HCI_RTS_BT	HCI_RTS_BT
41	HCI_TX_BT	HCI_TX_BT	HCI_TX_BT	HCI_TX_BT	HCI_TX_BT	HCI_TX_BT
42	HCI_RX_BT	HCI_RX_BT	HCI_RX_BT	HCI_RX_BT	HCI_RX_BT	HCI_RX_BT
43	NC	NC	NC	NC	NC	NC
44	AUD_FSYNC_BT	AUD_FSYNC_BT	AUD_FSYNC_BT	AUD_FSYNC_BT	AUD_FSYNC_BT	AUD_FSYNC_BT
45	AUD_CLK_BT	AUD_CLK_BT	AUD_CLK_BT	AUD_CLK_BT	AUD_CLK_BT	AUD_CLK_BT
46	AUD_IN_BT	AUD_IN_BT	AUD_IN_BT	AUD_IN_BT	AUD_IN_BT	AUD_IN_BT
47	AUD_OUT_BT	AUD_OUT_BT	AUD_OUT_BT	AUD_OUT_BT	AUD_OUT_BT	AUD_OUT_BT
48	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND
49	A: NC ; B: ANT3(2.4G)	A: NC ; B: ANT3(2.4G)	A: NC ; B: ANT3(2.4G)	A: NC ; B: ANT3(2.4G)	A: NC ; B: ANT3(2.4G)	A: NC ; B: ANT3(2.4G)
50	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND	A: NC ; B: GND
51	BT_HOST_WAKE_UP	BT_HOST_WAKE_UP	BT_HOST_WAKE_UP	BT_HOST_WAKE_UP	BT_HOST_WAKE_UP	BT_HOST_WAKE_UP
52	BT_WAKE_UP	BT_WAKE_UP	BT_WAKE_UP	BT_WAKE_UP	BT_WAKE_UP	BT_WAKE_UP
53	GND	GND	GND	GND	GND	GND
54	GND	GND	GND	GND	GND	GND
55	ANT2(2.4G)	ANT2(2.4G)	NC	NC	NC	NC
56	GND	GND	GND	GND	GND	GND

Table 3: Pinout Table

3.2 Pin Definition

Pin	Pin Name	I/O Type	Shut Down State	After Power Up	Description
1	ANT1(5G)	ANA			Antenna(5GHz) NC for CBM387and CBM287
2	GND	GND			GND
3	GND	GND			GND
4	ANT1(2.4G)	ANA			Antenna(2.4GHz)
5	GND	GND			GND
6	WL_EN	IN	PD	PD	WL enable high
7	BT_EN	IN	PD	PD	BT enable high
8	WL_RS232_RX	I/O	PD	PD	When IRQ_WL = 1 at power up
9	GNSS_PA_EN	I/O	PD	PD	NC if not used
10	GPS_PPS_OUT	I/O	PD	PD	Used to sync host, for host to provide data from external sensors. NC if not used
11	UART_DBG_WL	OUT	PU	PU	WLAN logger.
12	IRQ_WL	OUT	PD	0	SDIO available, interrupt out. Active high Need to force to 1 at power up to use WL_RS232_TX/RX
13	VBAT	POW			Main power supply, which can be a voltage from battery.
14	NC	ANA			NC
15	RTC_CLK	ANA			Slow clock. 32.768k
16	SDIO_D3_WL	I/O	HiZ	PU	WLAN SDIO Data bit 3 Changes state to PU at WL_EN or BT_EN assertion for card detect. Later disabled by the SW during init. Host must provide PU using 10 K resistor.
17	SDIO_D0_WL	I/O	HiZ	HiZ	WLAN SDIO Data bit 0 Host must provide PU using 10 K resistor.
18	SDIO_D2_WL	I/O	HiZ	HiZ	WLAN SDIO Data bit 2 Host must provide PU using 10 K resistor.
19	SDIO_D1_WL	I/O	HiZ	HiZ	WLAN SDIO Data bit 1 Host must provide PU using 10 K resistor.
20	SDIO_CMD_WL	IN	HiZ	HiZ	WLAN SDIO Command in Host must provide PU using 10 K resistor.
21	SDIO_CLK_WL	IN	HiZ	HiZ	WLAN SDIO Clock. Must be

					driven by the host.
22	VIO	POW			1.8V IO ring power supply voltage
23	NC	OUT	PD	PD	NC
24	NC				NC
25	NC				NC
26	NC				NC
27	NC				NC
28	NC				NC
29	EXT_LNA_EN_GNSS	OUT	PD	PD	External LNA enable. Option: WL_RS232_TX (when IRQ_WL = 1 at power up). NC if not used.
30	GND	GND			GND
31	GNSS_ANT	IN			GNSS RF in. NC if not used. (NC for CBM283, CBM286 and CBM287)
32	GND	GND			GND
33	NC				NC
34	UART_DBG_BT	OUT	PU	PU	BT debug (logger). NC if not used.
35	TIMESTAMP	IN	PD	PD	Option: wakeup GNSS functional block in sleep state. NC if not used. (NC for CBM283, CBM286 and CBM287)
36	IRQ_GNSS	OUT	PD	PD	GNSS IRQ to host. NC if not used. (NC for CBM283, CBM286 and CBM287)
37	PERIPH_I2C_SDA_GNSS	I/O	PU	PU	Debug I2C interface. Option: GPS_PA_EN. NC if not used. (NC for CBM283, CBM286 and CBM287)
38	PERIPH_I2C_SCL_GNSS	I/O	PU	PU	Debug I2C interface. NC if not used. (NC for CBM283, CBM286 and CBM287)
39	HCI_CTS_BT	IN	PU	PU	UART CTS from host. Shared HCI I/F. NC if not used. (NC for CBM283, CBM286 and CBM287)
40	HCI_RTS_BT	OUT	PU	PU	UART RTS to host. Shared HCI I/F. NC if not used.
41	HCI_TX_BT	OUT	PU	PU	UART TX to host. Shared HCI I/F. NC if not used.
42	HCI_RX_BT	IN	PU	PU	UART RX from host. Shared HCI

					I/F for BT and GNSS. NC if not used.
43	NC				NC
44	AUD_FSYNC_BT	OUT	PD	PD	BT PCM/I2S Frame sync. NC if not used.
45	AUD_CLK_BT	OUT	PD	PD	BT PCM/I2S Clock. NC if not used.
46	AUD_IN_BT	IN	PD	PD	BT PCM/I2S Data in. NC if not used.
47	AUD_OUT_BT	OUT	PD	PD	BT PCM/I2S Data out. NC if not used.
48	A: NC ; B: GND				A: NC ; B:GND
49	A: NC ; B: ANT3(2.4G)				A: NC ; B: ANT3(2.4G)
50	A: NC ; B: GND				A: NC ; B: GND
51	BT_HOST_WAKE_UP	I/O	PD	PD	Signal to wake up the host from BT. NC if not used.
52	BT_WAKE_UP	I/O	PD	PD	Bluetooth wakeup from host. NC if not used.
53	GND	GND			GND
54	GND	GND			GND
55	ANT2(2.4G)	ANA			Antenna(2.4GHz) NC for CBM386, CBM387, CBM286 and CBM287
56	GND	GND			GND

Table 4: Pin Definition

Note:

The Thermal (4*4=16) on the Bottom Layer needs to be connected to the GND Layer. Please use as many vias as possible from Top Layer to connect the Thermal to GND Layer.

4. Physical Interface

4.1 Power Management

4.1.1 Power-Up and Shut-Down States

The correct power-up and shut-down sequences must be followed to avoid damage to the device.

While VBAT or VIO or both are deasserted, no signals should be driven to the device. The only exception is the slow clock that is a fail-safe I/O.

While VBAT, VIO, and slow clock are fed to the device, but WL_EN is deasserted (low), the device is in SHUTDOWN state. In SHUTDOWN state all functional blocks, internal DC2DCs, clocks, and LDOs are disabled.

To perform the correct power-up sequence, assert (high) WL_EN. The internal DC2DCs, LDOs, and clock start to ramp and stabilize. Stable slow clock, VIO, and VBAT are prerequisites to the assertion of one of the enable signals.

To perform the correct shut-down sequence, deassert (low) WL_EN while all the supplies to the device (VBAT, VIO, and slow clock) are still stable and available. The supplies to the chip (VBAT and VIO) can be deasserted only after both enable signals are deasserted (low).

Figure 3 shows the general power scheme for the module, including the power-down sequence.

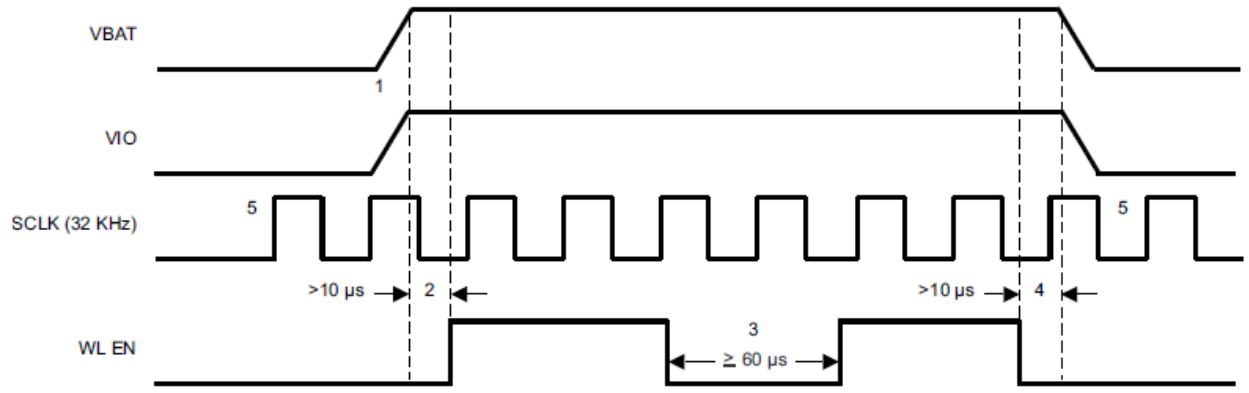

Figure 3: Power-Up System

NOTE: 1. Either VBAT or VIO can come up first.

2. VBAT and VIO supplies and slow clock (SCLK), must be stable prior to EN being asserted and at all times when the EN is active.

3. At least 60 µs is required between two successive device enables. The device is assumed to be in shutdown state during that period, meaning all enables to the device are LOW for that minimum duration.

4. EN must be deasserted at least 10 µs before VBAT or VIO supply can be lowered. (Order of supply turn off after EN shutdown is immaterial)

5. SCLK - Fail safe I/O

4.1.1.1 WLAN Power up Sequence

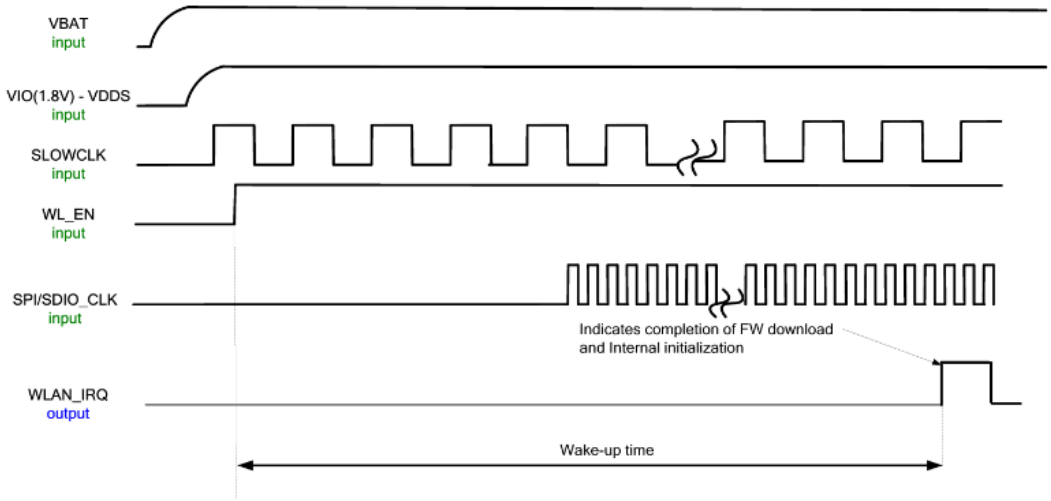

Figure 4: WLAN Power up Sequence

4.1.1.2 BT/BLE Power up Sequence

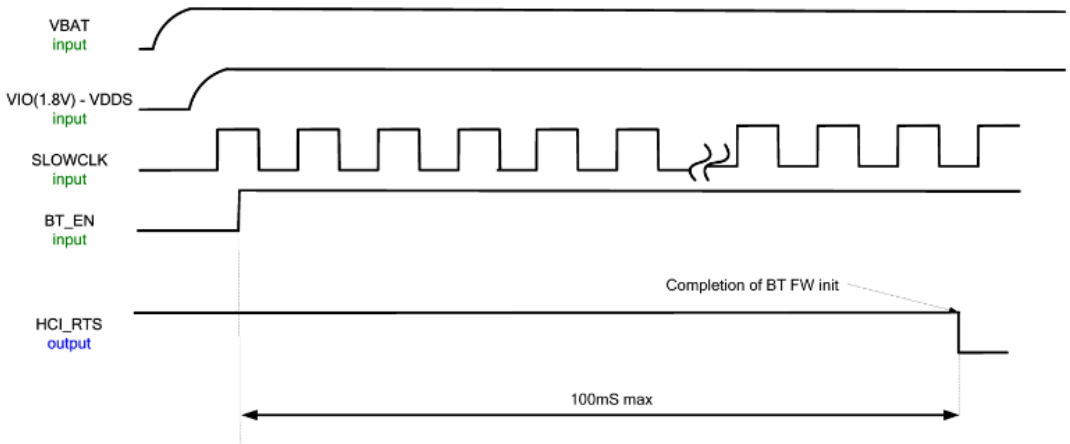

Figure 5: BT/BLE Power up Sequence

4.2 Host Interfaces

4.2.1 Device Host Interface Options

The following table summarizes the Host Controller interface options. All interfaces operate independently.

WLAN	Shared HCI for all functional blocks except WLAN	BT Voice/Audio
WLAN HS SDIO	Over UART	BT PCM

Table 5: Host Controller Interface options

The Device incorporates UART modules dedicated to the BT shared-transport Host Controller Interface (HCI) transport layer. The HCI interface is used to transport commands, events, ACL and synchronous data between the Bluetooth device and its host using HCI data packets.

The Device supports the following HCI transport layers (detected automatically when communication starts):

- UART transport layer: HCI four wire (H4) – Recommended interface

This acts as a shared transport for all functional blocks **except WLAN**.

4.2.2 WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the module- is a standard SDIO interface (meeting SDIO specification) and supports a maximum clock rate of 50MHz.

The Device SDIO also supports the following features of the SDIO V3 specification:

- 4 bit data bus
- Synchronous and Asynchronous In-Band-Interrupt
- Default and High-Speed (50MHz) timing
- Sleep/wake commands

SDIO timing specifications are given in Timing Specifications section.

4.2.3 HCI UART Shared Transport Layers for all functional blocks, except WLAN

The HCI UART supports most baud rates (including all PC rates) for all fast clock frequencies - up to maximum of 4 Mbps.

After power up the baud rate is set for 115.2 kbps, irrespective of fast clock frequency.

The baud rate can then be changed by using a vendor specific command. The Device responds with a Command Complete Event (still at 115.2 kbps), after which the baud rate change takes place.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions.
- Transmitter underflow detection.
- CTS/RTS hardware flow control.
- 4 wire (H4)

Parameter	Value
Bit rate	115.2 kbps
Data length	8 bits
Stop bit	1
Parity	None

Table 6: UART Default Setting

4.2.3.1 UART 4 Wire Interface - H4

The interface includes four signals: TXD, RXD, CTS and RTS. Flow control between the host and the Device is byte-wise by hardware.

Flow control is obtained by the following:

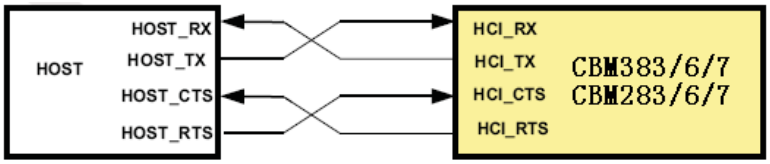

Figure 6: HCI UART Connection

When the UART RX buffer of the Device passes the “flow control” threshold, it will set the UART_RTS signal high to stop transmission from the host.

When the UART_CTS signal is set high, the Device will stop its transmission on the interface. In case HCI_CTS is set high in the middle of transmitting a byte, the Device will finish transmitting the byte and stop the transmission.

4.2.3.2 BT function Firmware Low Power Mode Protocols

The Device includes a mechanism that handles the transition between operating mode and deep sleep low-power mode. The protocol is done via the UART and is known as eHCILL (enhanced HCI Low Level) power management protocol.

This protocol is backward compatible with the BT HCILL Protocol, so a Host that implements the HCILL does not need to change anything in order to work with the Device. The "Enhanced" portion of the HCILL introduces changes that allow a simpler host implementation of this protocol.

4.2.4 BT Audio CODEC Interface

4.2.4.1 Overview

The CODEC interface is a fully dedicated programmable serial port, supporting the following:

- Two voice channels
- Master / slave modes
- Coding schemes: u-Law, A-Law, Linear, Transparent and SBC (for Assisted WBS operation)
- Long & short frames
- Different data sizes, order and positions
- Enlarged interface options to support a wider variety of Codecs

4.2.4.2 PCM Hardware Interface

The PCM interface is one implementation of the codec interface. It contains the following four lines:

- Clock--configurable direction (input or output)
- Frame Sync--configurable direction (input or output)
- Data In--Input
- Data Out--Output/Tri state

The Device can be either the master of the interface where it generates the clock and the frame-sync signals, or slave where it receives these two signals. The PCM interface is fully configured by means of a VS command.

For slave mode, clock input frequencies between 64KHz and 12 MHz are supported.

For master mode, the Device can generate any clock frequency between 64 kHz and 6 MHz.

4.2.4.3 PCM Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits, in 1 bit increments, when working with two channels, or up to 640 bits when using 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable with 1-clock (bit) resolution, and can be set independently (relative to the edge of the Frame Sync signal) for each channel.
- The Data_IN and Data_OUT bit order can be configured independently. For example; Data_IN can start with MSB while Data_OUT starts with LSB. Each channel is

separately configurable. The inverse bit order (i.e. LSB first) is supported only for sample sizes up to 24 bits.

- The data in and data out size do not necessarily have to be the same length.
- The Data_OUT line is configured as a 'high-Z' output between data words. Data_OUT can also be set for permanent high-Z, irrespective of data out. This allows the Device to be a bus slave in a multi-slave PCM environment. At power up, Data_OUT is configured as high-Z.

4.2.4.4 PCM Frame-Idle Period

The CODEC interface has the capability for frame-idle periods, where the PCM clock can "take a break" and become '0' at the end of the PCM frame, after all data has been transferred.

The Device supports frame-idle periods both as master and slave of the PCM bus.

When Device is the master of the interface, the frame-idle period is configurable. There are 2 configurable parameters:

- Clk_Idle_Start - Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes '0'.
- Clk_Idle_End - Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

e.g. For PCM clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90. Between each two-frame sync there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts 90-60=30 clock cycles. This means that the idle period ends 100-90=10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.

4.2.4.5 Two Channel PCM Bus Example

In the following figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame. (FT stands for Frame Timer).

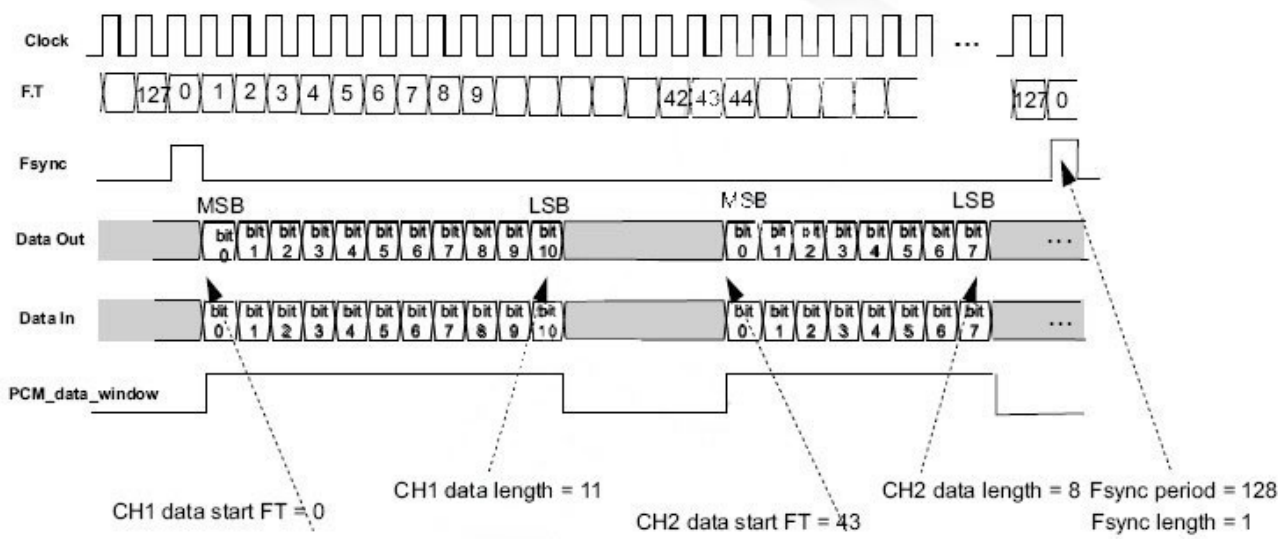

Figure 7: 2 Channels PCM Bus Timing

4.2.4.6 PCM Audio Encoding

The Device CODEC interface can use one of four audio coding patterns:

- A-Law (8-bit)
- μ-Law (8-bit)
- Linear (8 or 16-bit)
- SBC (16-bit)

Two BT voice channels are not supported when SBC encoding is selected

4.2.4.7 BT PCM Clock Mismatch Handling

In BT RX, the Device receives RF voice packets and writes these to the CODEC I/F. If the Device receives data faster than the CODEC I/F output allows, an overflow occurs. In this case, the Device BT function has 2 possible behavior modes: 'allow overflow' and 'don't allow overflow'.

- If overflow is allowed, the Device BT function continues receiving data and overwrites any data not yet sent to the CODEC.
- If overflow is not allowed, RF voice packets received when buffer is full, are discarded.

When the Bluetooth functional block is master on the PCM and slave on the Bluetooth network, the Bluetooth functional block can measure the drift between the two clocks and apply compensation to the PCM clock in order to avoid underrun and overrun scenarios

4.2.4.8 BT Inter-IC Sound (BT I2S over PCM bus)

The Device can be configured as an Inter-IC Sound (I2S) serial interface to a I2S CODEC device. In this mode, the Device audio CODEC interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 is used for the left channel

audio data and time slot 1 for the right channel audio data. Each time slot is configurable up to 40 serial clock cycles in length and the frame is configurable up to 80 serial clock cycles in length.

5. Clocks

5.1.1 Slow Clock / RTC clock

The slow clock is a free-running clock of 32.768 KHz which is supplied from an external clock source. It is connected to the RTC_CLK pin and is a digital square-wave signal in the range of 0-1.8V nom.

6. Functional Blocks

6.1 WLAN Functional Block

6.1.1 WLAN MAC

The Device MAC implements the IEEE standard 802.11 MAC sub-layer using both dedicated hardware and embedded firmware. The MAC hardware implements real-time functions, including access protocol management, encryption and decryption.

6.1.2 WLAN Baseband Processor

The Device baseband processor implements the IEEE 802.11a/b/g/n PHY sub layers and has been optimized to perform well in conditions of high multipath and noise.

6.1.3 WLAN RF Radio

The Device radio is a highly integrated radio processor designed for 802.11a/b/g/n applications, including internal front-end PAs, switches and filters.

6.1.4 Coexistence BT/BLE - WLAN - GNSS

The Device has been designed to support simultaneous operation of each of the major on-chip core functions. This operational coexistence is based on extensive frequency planning for each of the on-chip core functions, as well as a sophisticated MAC co-ordination scheme between Bluetooth and WLAN subsystems that allows operation in the same ISM frequency band.

6.2 Bluetooth Functional Block

6.2.1 BT Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. Received signal from the external antenna is input to an internal RF switch and a differential LNA (low-noise amplifier). This signal is then passed to a mixer which down-converts the signal to an IF, followed by a filter and amplifier. The signal is then quantized by a sigma-delta ADC. The quantized signal is further processed to reduce the interference level.

The demodulator digitally down-converts the signal to zero IF and recovers the data stream by an adaptive-decision mechanism. The demodulator includes EDR processing with state-of-the-art performance. It includes a maximum-likelihood sequence estimator (MLSE) for improved performance of basic-rate BR sensitivity, and adaptive equalization to enhance EDR modulation.

6.2.2 BT Transmitter

The transmitter is based on an all-digital sigma-delta PLL with a digitally controlled oscillator (DCO) as the RF frequency clock. The modulation is achieved by directly modulating the digital PLL. The power amplifier is also digitally controlled.

For EDR modulation, the transmitter uses a Polar-Modulation technique. In this mode, in addition to the frequency modulation that controls the direct-modulated ADPLL, an amplitude control modulates the PA, using the Digital-Transmitter block. This block receives the input bit-stream and converts these signals to phase-modulated control-words. The phase-modulated digital signal is then processed to provide frequency-modulation control to the ADPLL.

6.2.3 Class 1.5 Application.

Device provides on-chip support for Class 2 and Class 1.5 applications. Class 1.5 is the normal operating mode after the initialization script has been sent to the Device.

It is called Class 1.5 as Device can transmit more than 4dBm on any BT modulation.

Refer to Bluetooth RF Performance specifications at end of document for more information.

6.2.4 Advanced Audio features

The Device includes Audio and Voice Processor (AVPR) targeted for off-loading the host CPU from coding voice/audio samples when running A2DP and WBS profiles

6.2.4.1 Assisted Wideband (WB) speech

- Modified SBC including PLC for translating 16kHz PCM to/from 64kbps SBC frames
- Fully compliant with the BT SIG Wideband speech profile

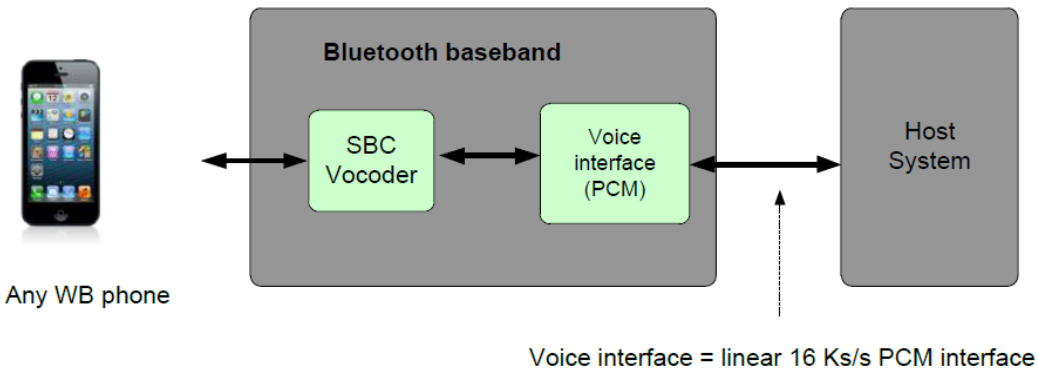

Figure 8: Device Wideband speech support

6.2.4.2 Assisted A2DP:

- SBC encode 44.1/48 kHz PCM to Low/Mid/High Quality A2DP stream
- Fully compliant with the BT SIG A2DP profile

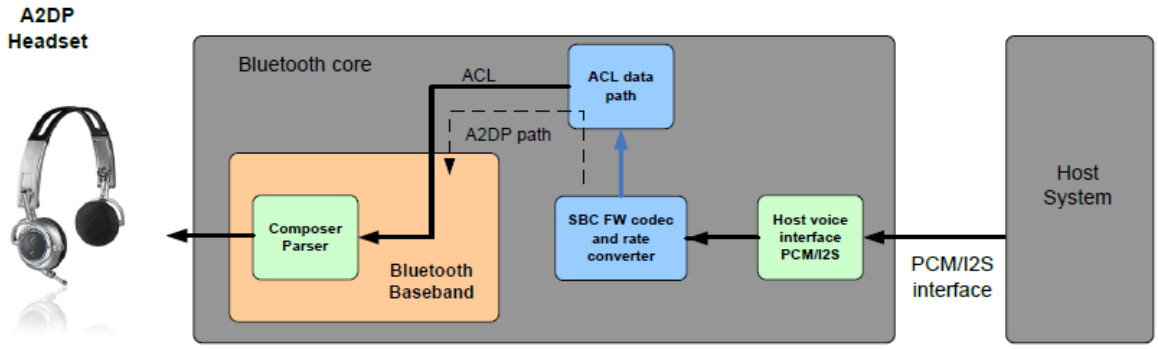

Figure 9: Device Assisted A2DP

6.3 GNSS Receiver Functional Block

GNSS implements a fully flexible multi satellite system GNSS receiver incorporating GPS, GLONASS, QZSS and SBAS technologies and provides a complete hardware and software solution. It includes an integrated RF, digital receiver and control subsystem. It is accessible from the host via the shared host interface over UART

The GNSSIP is composed of the five major subsystems:

- RF Frontend
- Digital Frontend
- Receiver Core
- Control Subsystem
- Power Management

6.3.1 RF Frontend

The RF Analog receives the RF signal from the antenna, passes it through a low noise amplifier, down-converts the signal to low IF and converts the signal to digital domain. The RF frontend supports both GPS and GLONASS bands.

6.3.2 Digital Frontend

The digital samples from the RF frontend are passed through a digital filter chain that down converts the signal to baseband and reduces the sample rate. The output of this module is sent to the receiver subsystem for further demodulation and decoding.

6.3.3 Receiver Core

This subsystem is the main hardware signal processing engine. The received data samples are passed through a dedicated engine that performs correlation followed by integration to enable separation of the signal from noise. The hardware consists of an acquisition engine, used for initial acquisition of satellites, and a tracking engine, used for tracking already acquired satellites. The data computed by this subsystem is stored in a memory; the data is subsequently read for further processing. The key features of the subsystem are:

- Support of up to 16 GPS and 9 GLONASS tracking channels
- Optimally shared data memory for storage of intermediate computation results

6.3.4 Control Subsystem

This module is responsible for controlling the entire digital and RF frontend after wakeup. The subsystem is built around an ARM core and includes a ROM for embedded FW , a RAM for data and program memory, OCP based interconnect, 2 channel DMA for host data transfer and host peripherals. Additionally, a few housekeeping modules and debug modules are part of this subsystem.

6.3.5 Power Management

This block is responsible for device wakeup, power management, clock and reset management during various GNSS operating states. The GNSS has 4 power states: Shutdown, Sleep, Idle and Active. The transition across these states is managed by handshake between the GNSS power management block and top level PRCM.

6.3.6 GNSS Firmware Architecture

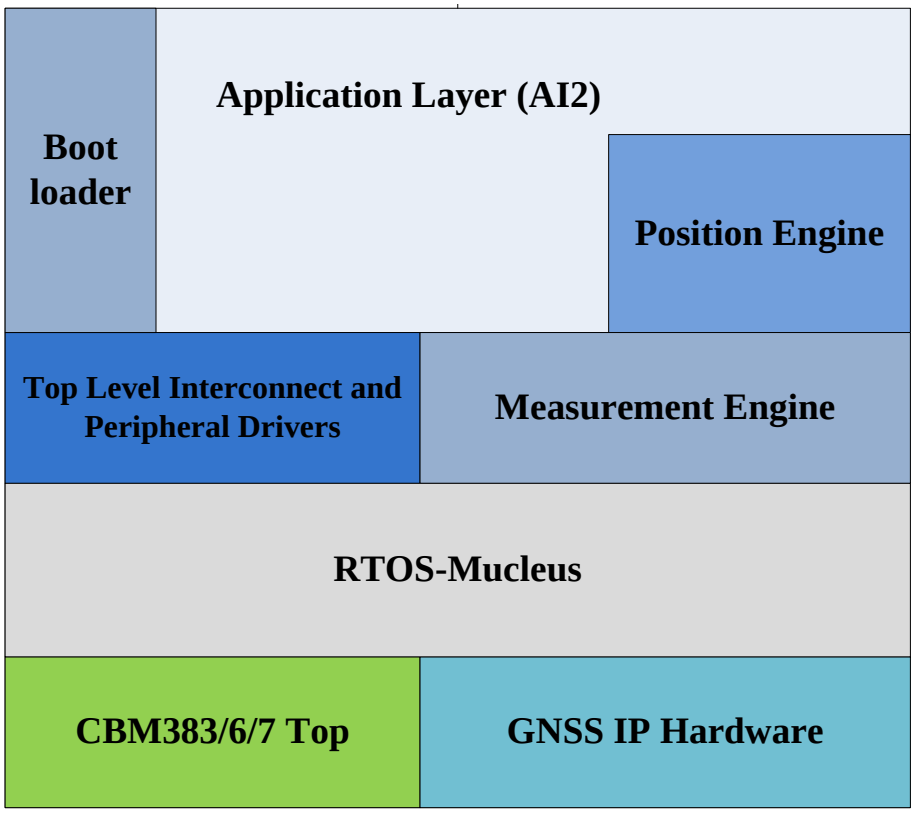

Figure 10: GNSS SW Architecture

The software components run on Nucleus RTOS. Following are the descriptions for key components:

- **Boot Loader:** This component is responsible for bringing up the software/system at power-up by configuring various blocks of digital and CM/PM section. Boot loader

component also allows downloading of any software service packs or external memory images.

- **Top-level Inter Connect and Peripheral Drivers:** This component is an ensemble of device drivers. This library offers device drivers for interface to the host (standalone/dedicated interface mode and shared interface mode) wakeup, watchdog, host wakeup, RTC time keeping, and RF control interface.
- **Application Layer Interface:** This component offers communication protocol functionality for host interface. It supports Air Interface Independent (AI2) protocol.
- **Measurement Engine (ME):** The Measurement Engine (ME) controls the entire search, acquisition, and measurement process. This component is responsible for generation of satellite measurement from hardware engine.
- **Position Engine (PE):** This component is responsible for generating location fixes from measurements and to collect/manage satellite data. The position engine component is also responsible for generation of steering for the measurement engine, which defines the satellite search space.

6.3.7 GNSS Modes of Operation

- The GNSS software engine supports following modes of operation:
- Autonomous

In autonomous operation, the GNSS engine performs a navigation computation without any assistance data. The GNSS engine supports hot, warm, and cold start operations.

6.3.8 External LNA Interface for GNSS

Noise figure of Device can be improved by using an external LNA. An external LNA, though not mandatory, may be required in the following cases:

- Higher jammer levels. In conditions where the level of interference/spurious is so high that a single SAW filter is not enough to meet the inter-mod levels specification, the external LNA helps. An additional SAW followed by the LNA helps improve jammer performance and also improves the noise figure of the system.
- Antenna placement. When the GNSS antenna is placed far away from the device, the extra path loss can be nullified by the external LNA kept closer to the antenna. However, this needs the power routing to the LNA to be longer and hence requires special attention.

The connection diagram for the external LNA is shown below.

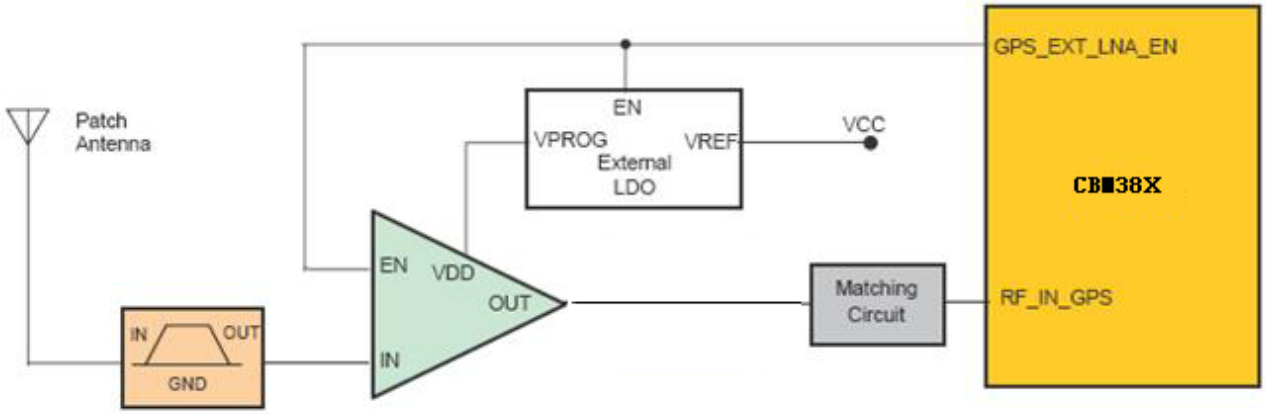

Figure 11: External LNA Powered Using External LDO

The enable signals of both external LNA and external LDO can be controlled using GNSS_EXT_LNA_EN signal (for power saving reasons).

In head unit infotainment systems the GPS signal might have to be routed from the far end of the housing to the front board where themodule will be mounted. Here is an example of how the signal routing can be achieved

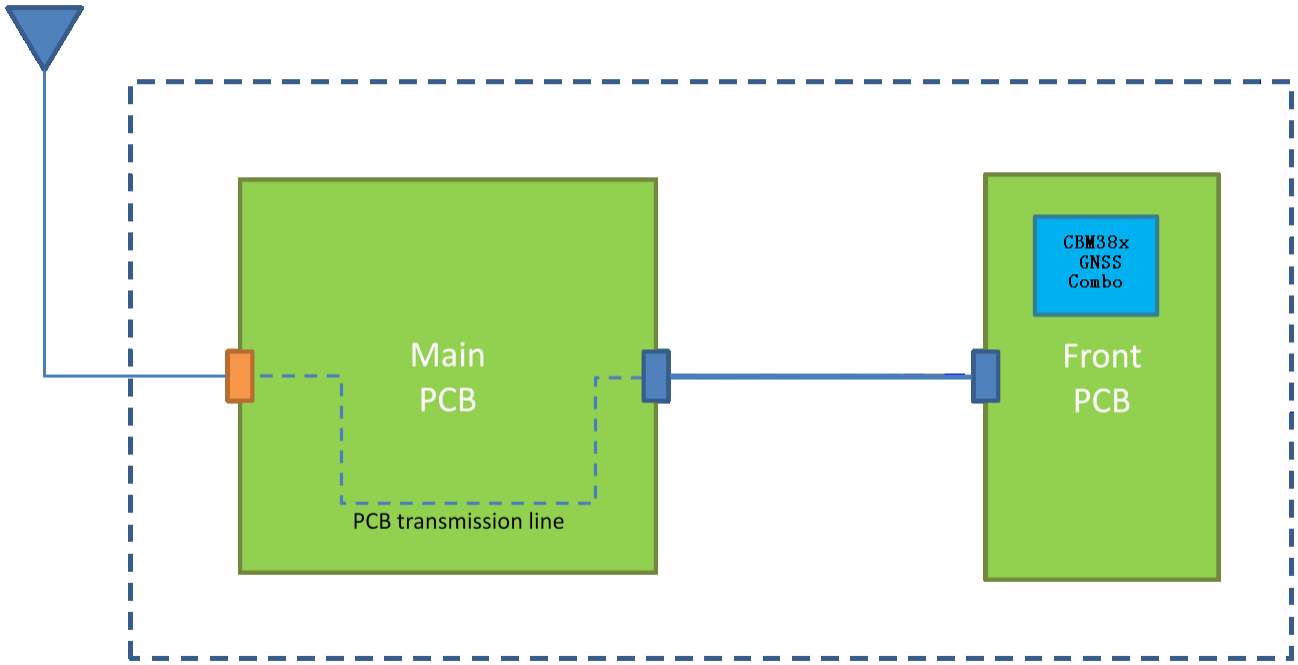

Figure 12: GPS Signal routing inside a head unit

7. Electrical Characteristic

7.1 Absolute Maximum Rating(1)

Parameter		Min	Max	Unit
VBAT		-0.5	5.5 (2)	V
VIO		-0.5	2.1	V
Input voltage to Analog pins (3)		-0.5	2.1	V
Input voltage to all other pins		-0.5	VDDS + 0.5V	V
Operating ambient temperature range		-40	+85 (4)	°C
Storage temperature range		-55	+125	°C
ESD Stress Voltage (5) To be updated after the completion of QUAL	Human Body Model (6)	1000	-	V
	Charged Device Model (7)	250	-	V

Table 7: Absolute Maximum Rating

1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) 5.5V up to 10s cumulative in 7 years, 5V cumulative to 250s, 4.8V cumulative to 2.33 years - all includes charging dips and peaks.

3) Analog pin: ANT1 (2.4G), ANT1 (5G), ANT2 (2.4G)

4) Operating free-air temperature range. The device can be reliably operated for 7 years at Tambient of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).

5) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

6) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.

7) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.

7.2 Recommended Operating Conditions

Parameter	Condition	Sym	Min	Max	Unit
Vbat	DC supply range for all modes		3	4.2	V
1.8 V IO ring power supply			1.62	1.95	
IO high-level input voltage		VIH	0.65 x VDD_IO	VDD_IO	
IO low-level input voltage		VIL	0	0.35 x VDD_IO	
Enable inputs high-level input		Vih_en	1.365	VDD_IO	
Enable inputs low-level input		Vil_en	0	0.4	
High-level output voltage	@ 4 mA	VOH	VDD_IO - 0.45	VDD_IO	
Low-level output voltage	@ 4 mA	VOL	0	0.45	
Input transitions time Tr/Tf from 10% to 90% (Digital IO) (1)		Tr/Tf	1	10	ns
Output rise time from 10% to 90% (Digital pins) (1)	CL < 25 pF	Tr		5.3	ns
Output fall time from 10% to 90% (Digital pins) (1)	CL < 25 pF	Tf		4.9	
Ambient operating temperature			-40	85	ºC
Thermal Characteristics	Junction-to-case	ΘJC	12.7		°C/W
	Junction-to-board	ΘJB	13.6		
	Junction-to-free	ΘJA	20.5		
	Junction-to-board	ΨJB	8.7		
Maximum power dissipation	WLAN operation			2.8	W
	Bluetooth operation			0.2	
	GNSS operation			0.1	

Table 8: Recommended Operating Conditions

1) Applies to all Digital lines except SDIO, UART, I2C, PCM and slow clock lines.
2) According to the JEDEC EIA/JESD 51 document

7.3 General Requirements and Operation

7.3.1 External Digital Slow Clock Requirements (-40 to +85°C)

Parameter	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy (Initial + temp + aging)	GNSS				±200	ppm
	WLAN, BT				±250	
Input transition time Tr/Tf -10% to 90%		Tr/Tf			100	ns
Frequency input duty cycle			15	50	85	%
Input voltage limits	Square wave, DC-coupled	Vih	0.65 x VDDS		VDDS	Vpeak
		Vil	0		0.35 x VDDS	
Input impedance			1			MΩ
Input capacitance					5	pF
Phase noise	1 kHz				-125	dBc/Hz
Jitter	Integrated over 300 - 15000 Hz				1Hz / 0.5nS	

Table 9: External Digital Slow Clock Requirements

7.3.2 Shutdown and Sleep Currents

Parameter	Power Supply Current	Min	Typ	25°C over process	Units
Shutdown mode All functions shut down.	Vbat		10	15	uA
	VIO		1.7	3	
WLAN sleep mode	Vbat		160	224	
BT sleep mode	Vbat		110	285	

Table 10: Shutdown and Sleep Currents

7.4 WLAN Performances

7.4.1 WLAN 2.4GHz RF Characteristics

7.4.1.1 WLAN 2.4GHz Receiver Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency range		2400		2480	MHz
Sensitivity - 20MHz bandwidth. - At < 10% PER limit MRC: If two antennas used (mimo device working in siso mode) receiving on both antennas will give 1-2 dB improvement.	1Mbps DSSS		-95		dBm
	11Mbps CCK		-87		
	12Mbps OFDM 1K		-88		
	54Mbps OFDM 1K		-74		
	MCS0 MM 4K		-89		
	MCS7 MM 4K		-71		
	MCS0 MM 4K 40MHz		-87		
	MCS7 MM 4K 40MHz		-68		
Max Input Level At < 10% PER limit	OFDM (11g/n)	-20	-8		dBm
	CCK	-4	0		
Adjacent ch rejection - sensitivity level +3 for OFDM - sensitivity level +6 for CCK	1 Mbps	-38			dB
	11 Mbps	-38			
	54 Mbps	2			
LO Leakage			-70		dBm

Table 11: WLAN 2.4GHz Receiver Characteristics

7.4.1.2 WLAN 2.4GHz Receiver Blocking Characteristics (Per Band)

The Device is designed to coexist with co-located cellular or other transmitters.

Parameter	Band	Min	Typ	Units
Blocking performance at specific bands For WLAN receiver de-sensing <= 1dB.	776 - 794 MHz (CDMA)	-5	15	dBm
	824 - 849 MHz (GMSK)	-5	15	
	824 - 849 MHz (EDGE)	-5	15	
	824 - 849 MHz (CDMA)	-5	15	
	880 - 915 MHz (GMSK)	15	18	
	880 - 915 MHz (EDGE)	15	18	
	1710 - 1785 MHz (GMSK)	-3	8	
	1710 - 1785 MHz (EDGE)	-3	8	
	1850 - 1910 MHz (GMSK)	-3	8	
	1850 - 1910 MHz (EDGE)	-3	8	
	1850 - 1910 MHz (CDMA)	-10	0	
	1850 - 1910 MHz (WCDMA)	-10	0	
	1920 - 1980 MHz (WCDMA)	-10	0	

Table 12: WLAN 2.4GHz Receiver Blocking Characteristics (Per Band)

7.4.1.3 WLAN 2.4GHz Transmitter Power

ANT1 (2.4G) measured at continuous TX

Parameter	Condition	ANT1(2.4G)			UNIT
		Min	Typ	Max	
Output Power. -Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM. -Power shown is per antenna. i.e. Total mimo power is power shown + 3dB.	1Mbps DSSS		16		dBm
	11Mbps CCK		16		
	12Mbps OFDM		16		
	54Mbps OFDM		13		
	MCS0 MM		15		
	MCS7 MM		13		
	MCS0 MM 40MHz		15		
	MCS7 MM 40MHz		13		
Output power accuracy			±2		dB
Output power resolution			0.125		dB

Table 13: WLAN 2.4GHz Transmitter Power

7.4.1.4 WLAN 2.4GHz Transmitter EVM

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency range		2412		2484	MHz
Return loss			-10		dB
Reference input impedance			50		Ω
EVM At max transmission power. EVM at lower powers will be less.	6 Mbps			-6	dB
	9 Mbps			-9	
	12Mbps			-11	
	18Mbps			-14	
	24Mbps			-17	
	36Mbps			-20	
	48Mbps			-23	
	54Mbps			-26	
	MCS0			-6	
	MCS1			-11	
	MCS2			-14	
	MCS3			-17	
	MCS4			-20	
	MCS5			-23	
	MCS6			-26	
	MCS7			-27	
	MCS8 (CBM283/CBM383)			-6	
	MCS9 (CBM283/CBM383)			-11	
	MCS10 (CBM283/CBM383)			-14	
	MCS11 (CBM283/CBM383)			-17	
	MCS12 (CBM283/CBM383)			-20	
	MCS13 (CBM283/CBM383)			-24	
	MCS14 (CBM283/CBM383)			-26	
	MCS15 (CBM283/CBM383)			-29	

Table 14: WLAN 2.4GHz Transmitter EVM

7.4.1.5 WLAN 2.4GHz Transmitter Out-of-band Emissions

Type	Band	Min	Typ	Max	Units
Out-of-band broadband emissions	<1GHz		-85		dBm/MHz
Out-of-band narrowband emissions	GLONASS 1596–1609 MHz		-88		dBm
Out-of-band broadband emissions	Second harmonic		-35		dBm/MHz
Out-of-band broadband emissions	Third Harmonic		-48		dBm/MHz
Out-of-band broadband emissions	Fourth Harmonic		-60		dBm/MHz

Table 15: WLAN 2.4GHz Transmitter Out-of-band Emissions

7.4.2 WLAN 5GHz Radio Characteristics (CBM383/CBM386/283/286 only)

7.4.2.1 WLAN 5GHz Rx RF Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency range		4910.0		5835.0	MHz
Sensitivity - 20MHz bandwidth. - At < 10% PER limit	6Mbps OFDM 1K		-89		dBm
	9Mbps OFDM 1K		-87		
	12Mbps OFDM 1K		-87		
	18Mbps OFDM 1K		-84		
	24Mbps OFDM 1K		-81		
	36Mbps OFDM 1K		-78		
	48Mbps OFDM 1K		-74		
	54Mbps OFDM 1K		-72		
	MCS0 MM 4K		-88		
	MCS1 MM 4K		-85		
	MCS2 MM 4K		-83		
	MCS3 MM 4K		-80		
	MCS4 MM 4K		-77		
	MCS5 MM 4K		-72		
	MCS6 MM 4K		-71		
	MCS7 MM 4K		-70		
	MCS0 MM 4K		-87		
	MCS7 MM 4K		-68		
Max Input Level	802.11a/n	-30			dBm
Adjacent Channel Rejection	OFDM54	2			dB
LO leakage			-50		dBm

Table 16: WLAN 5GHz Rx RF Characteristics

7.4.2.2 WLAN 5GHz Receiver Blocking Characteristics per Band

The Device is designed to coexist with co-located cellular transmitters.

Parameter	Baud	Min	Typ	Unit
Blocking Performance at other bands For WLAN receiver de- sensing <= 1dB.	776 - 794 MHz (CDMA)	30	34	dBm
	824 - 849 MHz (GMSK)	30	34	
	824 - 849 MHz (EDGE)	30	34	
	824 - 849 MHz (CDMA)	30	34	
	880 - 915 MHz (GMSK)	30	34	
	880 - 915 MHz (EDGE)	30	34	
	1710 - 1785 MHz (GMSK)	25	29	
	1710 - 1785 MHz (EDGE)	17	25	
	1850 - 1910 MHz (GMSK)	-18	9	
	1850 - 1910 MHz (EDGE)	-18	9	
	1850 - 1910 MHz (CDMA)	-18	9	
	1850 - 1910 MHz (WCDMA)	-18	9	
	1920 - 1980 MHz (WCDMA)	-2	8	

Table 17: WLAN 5GHz Receiver Blocking Characteristics per Band

7.4.2.3 WLAN 5GHz Transmitter Power

Parameter	Condition	Min	Typ	Max	Unit
Maximum RMS output power Output power measured at 1 dB from IEEE spectral mask or EVM.	6Mbps OFDM		17		dBm
	9Mbps OFDM		17		
	12Mbps OFDM		17		
	18Mbps OFDM		17		
	24Mbps OFDM		16		
	36Mbps OFDM		15		
	48Mbps OFDM		13		
	54Mbps OFDM		12		
	MCS0 MM		16		
	MCS1 MM 4K		16		
	MCS2 MM 4K		16		
	MCS3 MM 4K		16		
	MCS4 MM 4K		15		
	MCS5 MM 4K		14		
	MCS6 MM 4K		13		
	MCS7 MM 4K		13		
	MCS0 MM 40MHz		16		
	MCS7 MM 40MHz		13		
Output power accuracy			±2.5		dB
Output power resolution			0.125		dB

Table 18: WLAN 5GHz Transmitter Power

7.4.2.4 WLAN 5GHz Transmitter EVM

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency range		4910		5835	MHz
Return loss			-10		dB
Reference input impedance			50		Ω
EVM At max transmission power. EVM at lower powers will be less.	6 Mbps			-6	dB
	9 Mbps			-9	
	12Mbps			-11	
	18Mbps			-14	
	24Mbps			-17	
	36Mbps			-20	
	48Mbps			-23	
	54Mbps			-26	
	MCS0			-6	
	MCS1			-11	
	MCS2			-14	
	MCS3			-17	
	MCS4			-20	
	MCS5			-23	
	MCS6			-26	
	MCS7			-27	

Table 19: WLAN 5GHz Transmitter EVM

7.4.2.5 WLAN 5GHz Transmitter Out-of-band Emissions

Type	Band	Min	Typ	Max	Units
Out-of-band broadband emissions	RF X 4/3		-55		dBm/MHz
Out-of-band narrowband emissions	Second harmonic		-45		dBm/MHz
Out-of-band broadband emissions	Third harmonic		-50		dBm/MHz

Table 20: WLAN 5GHz Transmitter Out-of-band Emissions

7.5 BT Performance

7.5.1 BT BR, EDR Receiver Characteristics—In-Band Signals

Parameter	Condition		Min	Typ	Max	BT Spec	Unit
BT BR, EDR operation frequency range			2402		2480		MHz
BT BR, EDR channel				1			MHz
BT BR, EDR input				50			Ω
BT BR, EDR sensitivity (1) Dirty TX on	BR, BER = 0.1%			-91		-70	dBm
	EDR2, BER = 0.01%			-90		-70	
	EDR3, BER = 0.01%			-83		-70	
BT EDR BER floor at sensitivity + 10 dB, dirty TX off (for 1,600,000	EDR2		1e-6			1e-5	
	EDR3		1e-6			1e-5	
BT BR, EDR maximum useable input power	BR, BER = 0.1%		-5				dBm
	EDR2, BER = 0.01%		-12				
	EDR3, BER = 0.01%		-12				
BT BR intermodulation	Level of interferers For n = 3, 4,		-36	-30		-39	dBm
BT BR, EDR C/I performance Numbers show wanted-signal to interfering-signal ratio. Smaller numbers indicate better C/I performances (Image frequency = -1MHz)	BR, Co-channel					10	dB
	EDR, Co-channel	EDR2				12	
		EDR3				20	
	BR, adjacent ±1 MHz					-3	
	EDR, adjacent ±1 MHz, (image)	EDR2				-3	
		EDR3				2	
	BR, adjacent +2 MHz					-33	
	EDR, adjacent +2 MHz	EDR2				-33	
		EDR3				-28	
	BR, adjacent -2 MHz					-20	
	EDR, adjacent -2 MHz	EDR2				-20	
		EDR3				-13	
	BR, adjacent ≥I±3I MHz					-42	
	EDR, adjacent ≥I±3I MHz	EDR2				-42	
		EDR3				-36	
BT BR, EDR RF return				-10			dB

1) Sensitivity degradation up to -3dB may occur due to fast clock harmonics with dirty Tx on.

Table 21: BT BR, EDR Receiver Characteristics—In-Band Signals

7.5.2 BT Receiver Characteristics - General Blocking

Parameter	Condition	Min	Typ	Max	Unit
Blocking performance over full range, according to BT specification (1)	30-2000 MHz	10			dBm
	2000-2399 MHz	-27			
	2484-3000 MHz	-27			
	3-12.75 GHz	-10			

1) Exceptions taken out of the total 24 allowed in the BT spec.

Table 22: BT Receiver Characteristics - General Blocking

7.5.3 BT Receiver Characteristics - BR, EDR Blocking Per Band

Parameter	Band	Typ	Unit
Blocking performance for various cellular bands Hopping on. Wanted signal: -3dB from sensitivity, with modulated continuous blocking signal. BER = 0.1% for BT BR, 0.01% for BT EDR. PER = 1%	776-794 MHz (CDMA)	12	dBm
	824-849 MHz (GMSK) (1)	21	
	824-849 MHz (EDGE) (1)	13	
	824-849 MHz (CDMA, QPSK) (1)	12	
	880-915 MHz (GMSK)	10	
	880-915 MHz (EDGE)	9	
	1710-1785 MHz (GMSK)	16	
	1710-1785 MHz (EDGE)	1	
	1850-1910 MHz (GMSK)	1	
	1850-1910 MHz (EDGE)	0	
	1850-1910 MHz (CDMA, QPSK)	0	
	1850-1910 MHz (WCDMA, QPSK)	4	
	1920-1980 MHz (WCDMA, QPSK)	3	
	2400-2500 MHz (BT)	NA	
	2400-2500 MHz (WLAN)	NA	

1) Except for frequencies where [3 * F_BLOCKER] falls within the BT band (2400-2483.5 MHz)

Table 23: BT Receiver Characteristics - BR, EDR Blocking Per Band

7.5.4 BT Transmitter, BR

Parameter	Min	Typ	Max	BT Spec	Unit
BR RF output power (1)		10			dBm
BR Gain Control Range		30			dB
BR Power Control Step	2	5	8	2 to 8	
BR Adjacent Channel Power (2)			-35	≤ -20	dBm
BR Adjacent Channel Power (2)			-40	≤ -40	

1) Table shows maximum power. Reduced power available through VS command.

Table 24: BT Transmitter, BR

7.5.5 BT Transmitter, EDR

Parameter	Min	Typ	Max	BT Spec	Unit
EDR output power (1)		6			dBm
EDR Gain Control Range		30			dB
EDR Power Control Step	2	5	8	2 to 8	dB
EDR Adjacent Channel Power |M-N| = 1 (2)			-30	≤ -26	dBc
EDR Adjacent Channel Power |M-N| = 2 (2)			-23	≤ -20	dBm
EDR Adjacent Channel Power |M-N| > 2 (2)			-40	≤ -40	

1) Table shows default maximum power. Max power can be changed using VS command.

2) Assumes 3dB insertion loss on external filter and traces.

Table 25: BT Transmitter, EDR

7.5.6 BT Modulation, BR

Characteristics	Condition (1)		Performances			BT spec	Units
			Min	Typ	Max		
BR -20dB Bandwidth					995	≤1000	kHz
BR modulation characteristics	∆f1avg	Mod data = 4-ones, 4-zeros: 111100001111...	145		170	140 to 175	kHz
	∆f2max ≥ limit for at least 99.9% of all	Mod data = 1010101...	120			> 115	kHz
	∆f2avg / ∆f1avg		85			> 80	%
BR carrier frequency drift	One slot packet		-25		25	< ±25	kHz
	Three and five slot packet		-35		35	< ±40	kHz
BR drift rate	lfk+5 – fkl , k = 0 …. max				15	< 20	kHz/ 50µs
BR initial carrier frequency tolerance	f0 – fTX		-25		25	< ±75	kHz

1) Performance figures at maximum power

Table 26: BT Modulation, BR

7.5.7 BT Modulation, EDR

Parameter (1)	Condition	Min	Typ	Max	BT	Unit
EDR Carrier frequency		-5		5	≤10	kHz
EDR Initial Carrier Frequency Tolerance		-25		25	±75	kHz
EDR RMS DEVM	EDR2			15	20	%
	EDR3			10	13	%
EDR 99% DEVM	EDR2			30	30	%
	EDR3			20	20	%
EDR Peak DEVM	EDR2			25	35	%
	EDR3			25	25	%

1）Performance figures at maximum power

Table 27: BT Modulation, EDR

7.5.8 BT BR, EDR Transceiver – Emissions

Characteristics (1)	Condition	Performances			Units
		Min	Typ	Max	
Bluetooth BR, EDR out-of-band 1598–1607 MHz –33 dBm/MHz emission	1598–1607 MHz –33 dBm/MHz emission (GLONASS)(1)		-13		dBm/MHz
BT harmonics	2nd harmonic		-9		dBm/Mhz
	3rd harmonic		-20		dBm/MHz
	4th harmonic		-30		dBm/MHz

（1）Spur from Bluetooth LO on 2/3*RF_FREQ in the GLONASS band is canceled by the AFH mechanism while GNSS is enabled

Table 28: BT BR, EDR Transceiver – Emissions

7.5.9 BT BR Transceiver – Spurs

Characteristics (1)	Condition (2)		Performances			Units
			Min	Typ	Max	
BT out-of-band spurs	76-108 MHz (FM)	BR		-77	-68	dBm
	746-768 MHz (WCDMA)			-79	-70	dBm
	869-894 MHz (WCDMA, GSM)			-77	-68	dBm
	925-960 MHz (E-GSM)			-77	-67	dBm
	1570-1580 MHz (GPS)			-72	-60	dBm
	1598-1607 MHz (GLONASS) (3)			-74	-58	dBm
	1805-1880 MHz (DCS, WCDMA)			-72	-62	dBm
	1930-1990 MHz (PCS)			-70	-61	dBm
	2110-2170 MHz (WCDMA)			-59	-49	dBm

1) Meets FCC and ETSI requirements with suitable external filter
2) Performance figures at maximum power
3) Except for frequencies that corresponds to 2*RF_FREQ/3

Table 29: BT BR Transceiver – Spurs

7.5.10 BT EDR Transceiver – Spurs

Characteristics (1)	Condition (2)		Performances			Units
			Min	Typ	Max	
BT out-of-band spurs	76-108 MHz (FM)	EDR		-82	-70	dBm
	746-768 MHz (WCDMA)			-87	-78	dBm
	869-894 MHz (WCDMA, GSM)			-85	-70	dBm
	925-960 MHz (E-GSM)			-84	-74	dBm
	1570-1580 MHz (GPS)			-79	-60	dBm
	1598-1607 MHz (GLONASS) (3)			-78	-58	dBm
	1805-1880 MHz (DCS, WCDMA)			-76	-66	dBm
	1930-1990 MHz (PCS)			-74	-65	dBm
	2110-2170 MHz (WCDMA)			-63	-51	dBm

1) Meets FCC and ETSI requirements with suitable external filter
2) Performance figures at maximum power
3) Except for frequencies that corresponds to 2*RF_FREQ/3

Table 30: BT EDR Transceiver – Spurs

7.5.11 BT Dynamic Currents

BR = 14.5dBm, EDR = 10dBm.

Use Case (1) (2)	Typ	Units
BR Voice HV3 + sniff	11.6	mA
EDR Voice 2-EV3 no retrans. + sniff	5.9	mA
Sniff 1 attempt 1.28s	178	uA
EDR A2DP EDR2 (master) SBC high quality – 345Kbs	10.4	mA
EDR A2DP EDR2 (master) MP3 high quality – 192Kbs	7.5	mA
Full throughput ACL RX: RX-2DH5 (3) (4)	18	mA
Full throughput BR ACL TX: TX-DH5 (4)	50	mA
Full throughput EDR ACL TX: TX-2DH5 (4)	33	mA
Page or inquiry 1.28s/11.25ms	253	uA
P&I Scan (P=1.28/I=2.56)	332	uA

1) BT role in all scenarios is Slave, except for A2DP
2) CL1P5 PA connected to Vbat, 3.7V
3) ACL RX has same current in all modulations
4) Full throughput assume data transfer in one direction

Table 31: BT Dynamic Currents

7.6 BT LE Performance

7.6.1 BT LE Receiver Characteristics - In-Band Signals

Parameter	Condition (2)	Min	Typ	Max	BLE	Unit
BT LE Operation frequency range		2402		2480		MHz
BT LE Channel spacing			2			MHz
BT LE Input impedance			50			Ω
BT LE Sensitivity (1) Dirty Tx on			-91		≤ -70	dBm
BT LE Maximum useable		-5			≥ -10	dBm
BT LE Intermodulation	Level of interferers. For n = 3,	-36			≥ -50	dBm
BT LE C/I performance Note: Numbers show wanted signal-to- interfering signal ratio. Smaller numbers indicate better C/I performance.	LE, co-channel			12	≤ 21	dB
	LE, adjacent ±1MHz			0	≤ 15	
	LE, adjacent +2MHz			-38	≤ -17	
	LE, adjacent –2MHz			-15	≤ -15	
	LE, adjacent ≥ |±3|MHz			-40	≤ -27	

1) Sensitivity degradation up to -3dB may occur due to fast clock harmonics.
2) BER of 0.1% corresponds to PER of 30.8% for a minimum of 1500 transmitted packets, according to BT LE test spec

Table 32: BT LE Receiver Characteristics - In-Band Signals

7.6.2 BT LE Receiver Characteristics - General Blocking

Parameter	Condition	Min	Typ	Max	BLE	Unit
BT LE Blocking performance over full range, according to LE specification (1)	30–2000MHz	–10			≥ –30	dBm
	2000–2399MHz	–35			≥ –35	
	2484–3000MHz	–35			≥ –35	
	3–12.75GHz	–30			≥ –30	

1) Exceptions taken out of the total 10 allowed for fbf_1, according to the BT LE Spec

Table 33: BT LE Receiver Characteristics - General Blocking

7.6.3 BT LE Receiver Characteristics - Blocking per Band

Same as BT BR with following conditions:

- Hopping off.
- Desired signal: -3dB from sensitivity, with modulated continuous blocking signal. PER = 30.8%

7.6.4 BT LE Transmitter Characteristics

Parameter	Min	Typ	Max	BT LE Spec	Unit
BT LE RF output power(1)		10		≤10	dBm
BT LE Adjacent Channel Power (2)			-43	≤ –20	dBm
BT LE Adjacent Channel Power (2)			-46	≤ –30	

1) The maximum BLE power can be reduced using a vendor specific command. The extra margin is offered to optionally compensate for design losses like trace and filter losses and achieve the maximum allowed output power at system level.

2) Assumes 3dB insertion loss on external filter and traces

Table 34: BT LE Transmitter Characteristics

7.6.5 BT LE Modulation Characteristics

Characteristics	Condition (1)		Performances			BT Spec	Units
			Min	Typ	Max		
BT LE modulation characteristics	∆f1avg	Mod data = 4-ones, 4-zeros: 111100001111...	240	250	270	225 to 275	kHz
	∆f2max ≥ limit for at least 99.9% of all ∆f2max	Mod data = 1010101...	195			≥185	kHz
	∆f2avg / ∆f1avg		85			≥80	%
BT LE carrier frequency drift	lf0 – fnl , n = 2,3 …. K		-25		25	±50	kHz
BT LE drift rate	lf1 – f0l and lfn – fn-5l ,n = 6,7…. K				15	≤20	kHz/ 50µs
LE initial carrier frequency tolerance	fn – fTX		-25		25	±100	kHz

1) Performance figures at maximum power

Table 35: BT LE Modulation Characteristics

7.6.6 BT LE Transceiver - Emissions

Same as BT BR

7.6.7 BT LE Transceiver - Spurs

Same as BT BR

7.6.8 BT LE Currents

Use Case(1)	Output [dBm]	Typ	Units
Advertising, non-connectable (2)	10	131	uA
Advertising, discoverable (2)	10	143	uA
Scanning (3)	10	266	uA
Connected, master role, 1.28sec conn. interval (4)	10	124	uA
Connected, slave role, 1.28sec conn. interval (4)	10	132	uA

1) CL1p% PA connected to Vbat, 3.7V
2) Advertising in all 3 channels, 1.28sec advertising interval, 15 Bytes advertise data.
3) Listening to a single frequency per window, 1.28sec scan interval, 11.25msec scan window.
4) Zero Slave connection latency Empty Tx/Rx LL packets.

Table 36: BT LE Currents

7.7 GNSS Performance

7.7.1 Sensitivity and TTFF

Parameter	Condition	Min	Typ	Max	Unit
Autonomous Cold Start Sensitivity			-145		dBm
A-GPS Sensitivity (coarse time)			-156		dBm
Hot Start Sensitivity			-158		dBm
Tracking Sensitivity			-161		dBm
Autonomous Cold Start TTFF at -130dBm			28		s
Autonomous Cold Start TTFF at -142dBm			41		s
Hot start TTFF @-130dBm			1.2		s

All figures reported at chip input in internal LNA mode

Table 37: Sensitivity and TTFF

7.7.2 GNSS RF Chain Performance (Internal LNA Mode)

7.7.2.1 GNSS NF and Gain Specifications

Parameter	Condition	Min	Typ	Max	Unit
NF in GPS Band	Measured at the VGA Output		2.5	3.5	dB
NF in GLONASS Band	Measured at the VGA Output		2.6	4.0	dB
Input 1-dB compression point	Measured with a 1575.42-MHz tone at LNA I/P, with VGA gain set at minimum	-80			dBm
Input return loss	Single-ended with external matching		-12		dB
LO leakage	Measured at RF input port on 50-W		-70		dBm
Maximum RF input level	Maximum RF level before destruction	0			dBm

Table 38: GNSS NF and Gain Specifications

7.7.2.2 GNSS Linearity Specifications in Internal LNA Mode

Linearity specifications to be met by devices with worst-case noise figure.

Parameter	Condition	Min	Typ	Max	Unit
IIP3 at 915 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 914 MHz at -33 dBm	-22			dBm
IIP3 at 1710 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2 1710 MHz at -43 dBm	-24			dBm
IIP3 at 1850 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 1850 MHz at -38 dBm	-22			dBm
IIP3 at 2402 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 2402 MHz at -22 dBm	-18			dBm
IIP3 at 4900 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 4900 MHz at -4 dBm	2			dBm
IIP2 at 915 MHz	Feed: Tone 1: 910 MHz at -39 dBm Tone 2: 914.092 MHz at -39 dBm	23			dBm
IIP2 at 1710 MHz	Feed: Tone 1: 1710 MHz at -43 dBm Tone 2: 1714.092 MHz at -43 dBm	20			dBm
IIP2 at 1850 MHz	Feed: Tone 1: 1850 MHz at -38 dBm Tone 2: 1854.092 MHz at -38 dBm	31			dBm

IIP2 at 2402 MHz	Feed: Tone 1: 2402 MHz at -28 dBm Tone 2: 2406.092 MHz at -28 dBm	35			dBm
IIP2 at 2500 MHz	Feed: Tone 1: 2500 MHz at -33 dBm Tone 2: 2504.092 MHz at -33 dBm	41			dBm
IIP2 at 4900 MHz	Feed: Tone 1: 4900 MHz at -3 dBm Tone 2: 4904.092 MHz at -3 dBm	84			dBm

Table 39: GNSS Linearity Specifications in Internal LNA Mode

7.7.3 GNSS RF Chain Performance (External LNA Mode)

7.7.3.1 GNSS NF and Gain Specifications in External LNA Mode

Parameter	Condition	Min	Typ	Max	Unit
NF in GPS Band	Measured at the VGA Output		4		dB
NF in GLONASS Band	Measured at the VGA Output		4		dB
Input 1-dB compression point	Measured with a 1575.42-MHz tone at LNA I/P, with VGA gain set at minimum	-70			dBm
Input return loss	Single-ended with external matching		-12	-6	dB
LO leakage	Measured at RF input port on 50-W termination with matching network		-70		dBm
Maximum RF input level at LNA_IN pin	Maximum RF level before destruction	0			dBm

Table 40: GNSS NF and Gain Specifications in External LNA Mode

7.7.3.2 GNSS Linearity Specifications in External LNA Mode

Parameter	Condition	Min	Typ	Max	Unit
IIP3 at 915 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 914 MHz at -41 dBm	-29			dBm
IIP3 at 1710 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2 1710 MHz at -50 dBm	-31			dBm
IIP3 at 1850 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 1850 MHz at -47 dBm	-31			dBm
IIP3 at 2402 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 2402 MHz at -28 dBm	-18			dBm

IIP3 at 4900 MHz	Feed: Tone 1: 1575.42 MHz at -90 dBm Tone 2: 4900 MHz at -34 dBm	-30			dBm
IIP2 at 915 MHz	Feed: Tone 1: 910 MHz at -46 dBm Tone 2: 914.092 MHz at -46 dBm	8			dBm
IIP2 at 1710 MHz	Feed: Tone 1: 1710 MHz at -50 dBm Tone 2: 1714.092 MHz at -50 dBm	14			dBm
IIP2 at 1850 MHz	Feed: Tone 1: 1850 MHz at -47 dBm Tone 2: 1854.092 MHz at -47 dBm	14			dBm
IIP2 at 2402 MHz	Feed: Tone 1: 2402 MHz at -31 dBm Tone 2: 2406.092 MHz at -31 dBm	21			dBm
IIP2 at 2500 MHz	Feed: Tone 1: 2500 MHz at -31 dBm Tone 2: 2504.092 MHz at -31 dBm	36			dBm
IIP2 at 4900 MHz	Feed: Tone 1: 4900 MHz at -34 dBm Tone 2: 4904.092 MHz at -34 dBm	20			dBm

Table 41: GNSS Linearity Specifications in External LNA Mode

7.7.3.3 GNSS VGA Performance (Internal and External LNA Modes)

Parameter	Condition	Min	Typ	Max	Unit
Minimum gain				0	dB
Maximum gain		26			dB
Step size			2		dB
Step error				1	dB

Table 42: GNSS VGA Performance (Internal and External LNA Modes)

7.7.4 GNSS Currents

Parameter	Condition	Vbat Current (Typ)	Unit
Sleep	Lowest possible power consumption state in which all GNSS information is retained to provide a hot fix on wakeup	0.22	mA
Idle	Transition mode between active, and sleep modes all other blocks turned off.	2.0	mA
Acquisition	Power state when receiver is active and looking to acquire the satellite signal.	24	mA
Tracking	Power state where receiver is active and HW is optimally used for satellite tracking and making location fixes.	21	mA

Table 43: GNSS Currents

7.8 Interface Timing Characteristics

7.8.1 UART Timing

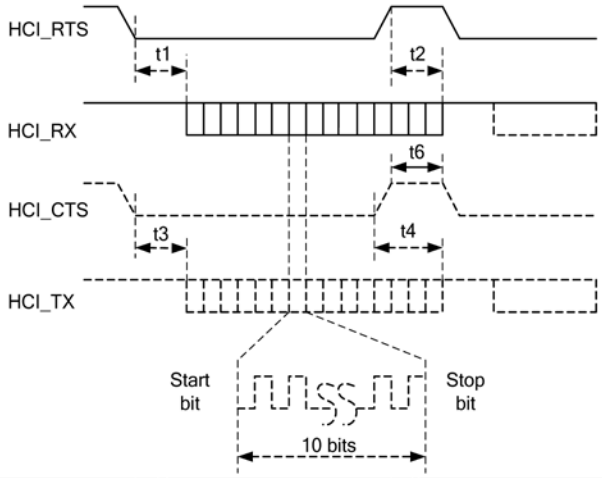

Figure 13: UART Timing Diagram

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Baud rate			37.5		4364	Kbps
Baud rate accuracy per	Receive/Transmit		-2.5		+1.5	%
Baud rate accuracy per bit	Receive/Transmit		-12.5		+12.5	%
CTS low to TX_DATA on		t3	0	2		□s
CTS high to TX_DATA off	Hardware flow	t4			1	Byte

CTS High Pulse Width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		□s
RTS high to RX_DATA off	Interrupt set to 1/4	t2			16	Bytes

Table 44: UART Timing Diagram

STR - Start bit
D0..Dn - Data bits (LSB first)
PAR - Parity bit (if used)
STP - Stop bit

7.8.2 SDIO timing specifications

7.8.2.1 SDIO Switching Characteristics - Default Rate Input and Output

Over recommended operating conditions Parameters for maximum clock frequency

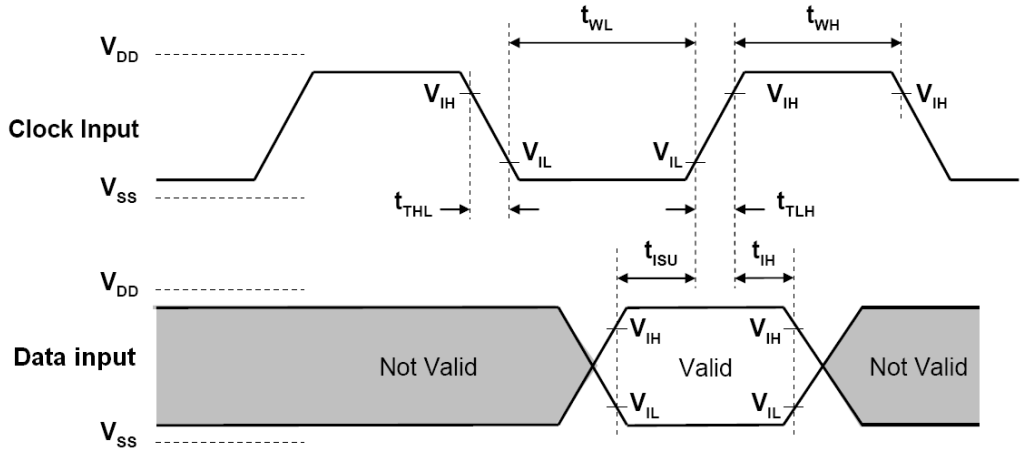

Figure 14: SDIO Default Input Timing

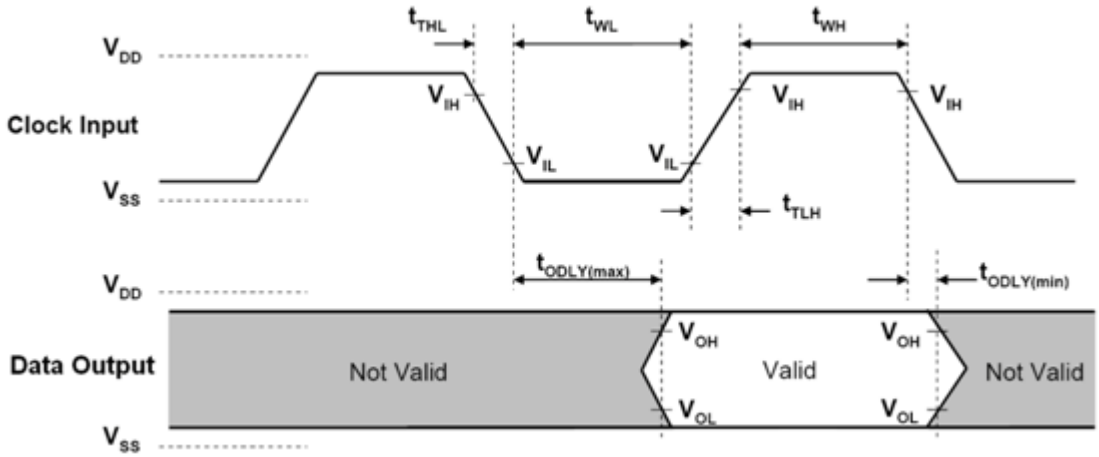

Figure 15: SDIO Default Output Timing

Parameter		Min	Max	Unit
fclock	Clock frequency, CLK	0	26	MHz
DC	Low/high duty cycle	40	60	%
tTLH	Rise time, CLK		10	ns
tTHL	Fall time, CLK		10	ns
tISU	Setup time, input valid before CLK ↑	3		ns
tIH	Hold time, input valid after CLK ↑	2		ns
tODLY	Delay time, CLK ↓ to output valid	2.5	14.8	ns
Cl	Capacitive load on outputs		15	pF

Note: Option to change data out clock edge from falling edge (default) to rising edge, by setting configuration bit.

Table 45: SDIO Switching Characteristics - Default Rate Input and Output

7.8.2.2 SDIO Switching Characteristics - High Rate

Over recommended operating conditions

Parameters for maximum clock frequency

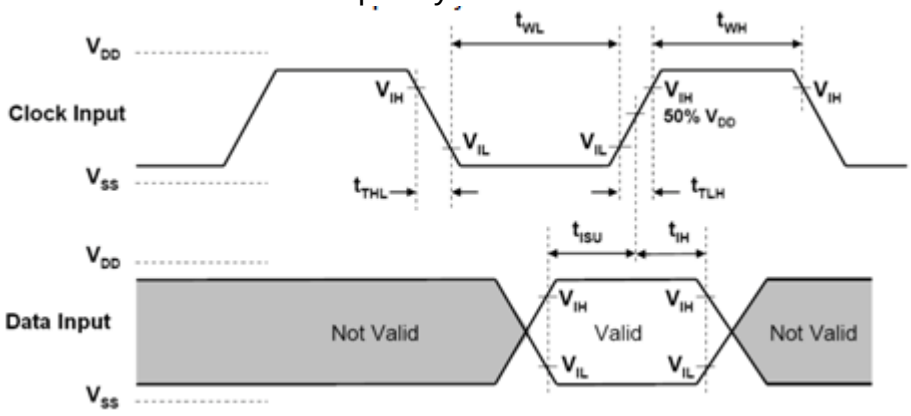

Figure 16: SDIO HS Input Timing

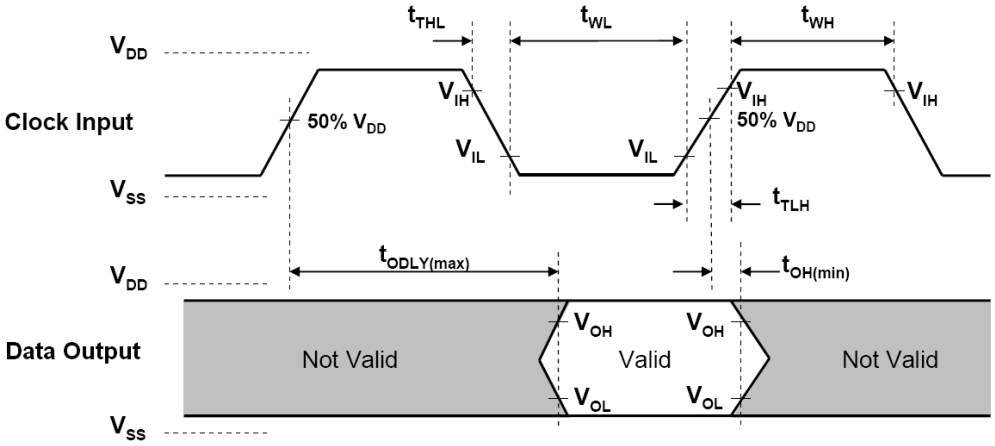

Figure 17: SDIO HS Output Timing

Parameter		Min	Max	Unit
fclock	Clock frequency, CLK	0	50	MHz
DC	Low/high duty cycle	40	60	%
tTLH	Rise time, CLK		3	ns
tTHL	Fall time, CLK		3	ns
tISU	Setup time, input valid before CLK ↑	3		ns
tIH	Hold time, input valid after CLK ↑	2		ns
tODLY	Delay time, CLK ↑ to output valid	2.5	14	ns
Cl	Capacitive load on outputs		10	pF

Table 46: SDIO Switching Characteristics - High Rate

7.8.3 BT Codec/PCM (Audio) Timing Specifications

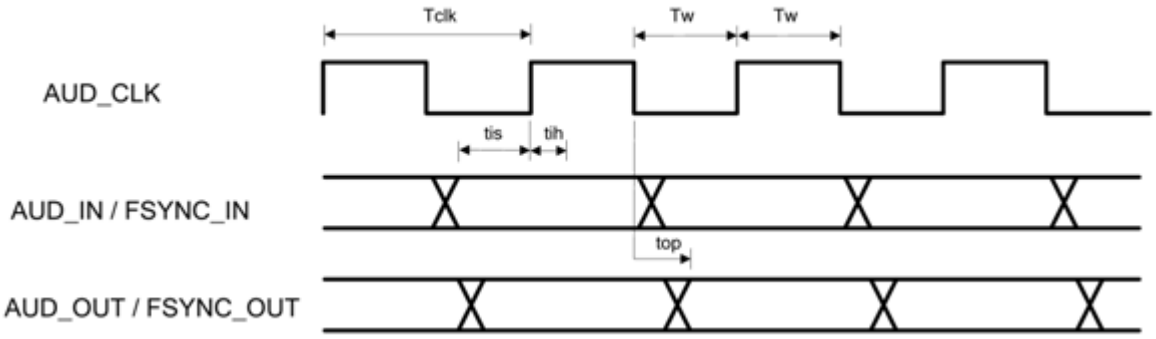

Figure 18: PCM Interface Timing

7.8.3.1 PCM Master

Parameter	Symbol	Min	Max	Unit
Cycle time	Tclk	166.67 (6.144 MHz)	15625 (64 kHz)	ns
High or low pulse width	Tw	35% of Tclk min		
AUD_IN setup time	tis	10.6		
AUD_IN hold time	tih	0		
AUD_OUT propagation time	top	0	15	
AUD_FSYNC_OUT propagation	top	0	15	
Capacitive loading on outputs	Cl		40	pF

Table 47: PCM Master

7.8.3.2 PCM Slave

Parameter	Symbol	Min	Max	Unit
Cycle time	Tclk	81 (12.288MHz)		ns
High or low pulse width	Tw	35% of Tclk min		
AUD_IN setup time	tis	5		
AUD_IN hold time	tih	0		
AUD_FSYNC setup time	tis	5		

AUD_FSYNC hold time	tih	0		
AUD_OUT propagation time	top	0	19	
Capacitive loading on outputs	Cl		40	pF

Table 48: PCM Slave

7.9 ESD and reliability test

Test Item	Test Conditions	Test Results
ESD	working state, Human Body Model 1000V, every pin contacts discharge three times,and interval is 3s.	Pass
High Temp Storage	without electricity, 85 ℃, 48h	Pass
Low Temp Storage	Without electricity, -40℃, 24h	Pass
Temperature alternation	working state, high temp 85℃ 110min, low temp -40℃ 90min, 30 cycles.	Pass
Temperature ictus	without electricity, high temp 85 ℃20min, low temp -40℃ 20min, High and low temperature conversion time is less than 30s, 100 cycles.	Pass
Damp-heat cycles	working state, low temp 25℃ humidity 97%, high temp 55℃ humidity 93%, 24h a cycle, 6 cycles.	Pass

Table 49: ESD and reliability test

8. Reference Design

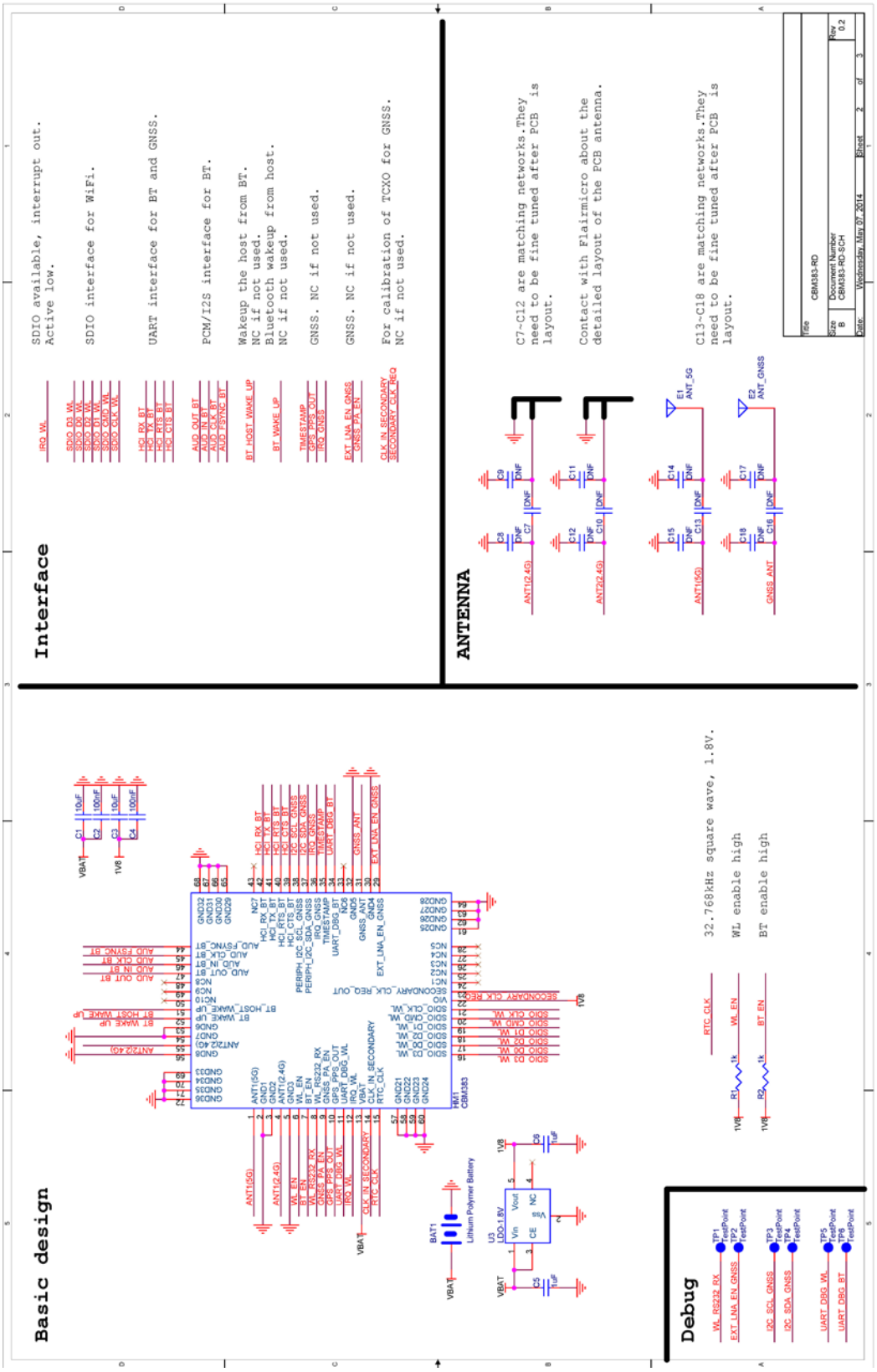

Figure 19: Reference Design

9. Mechanical Characteristic

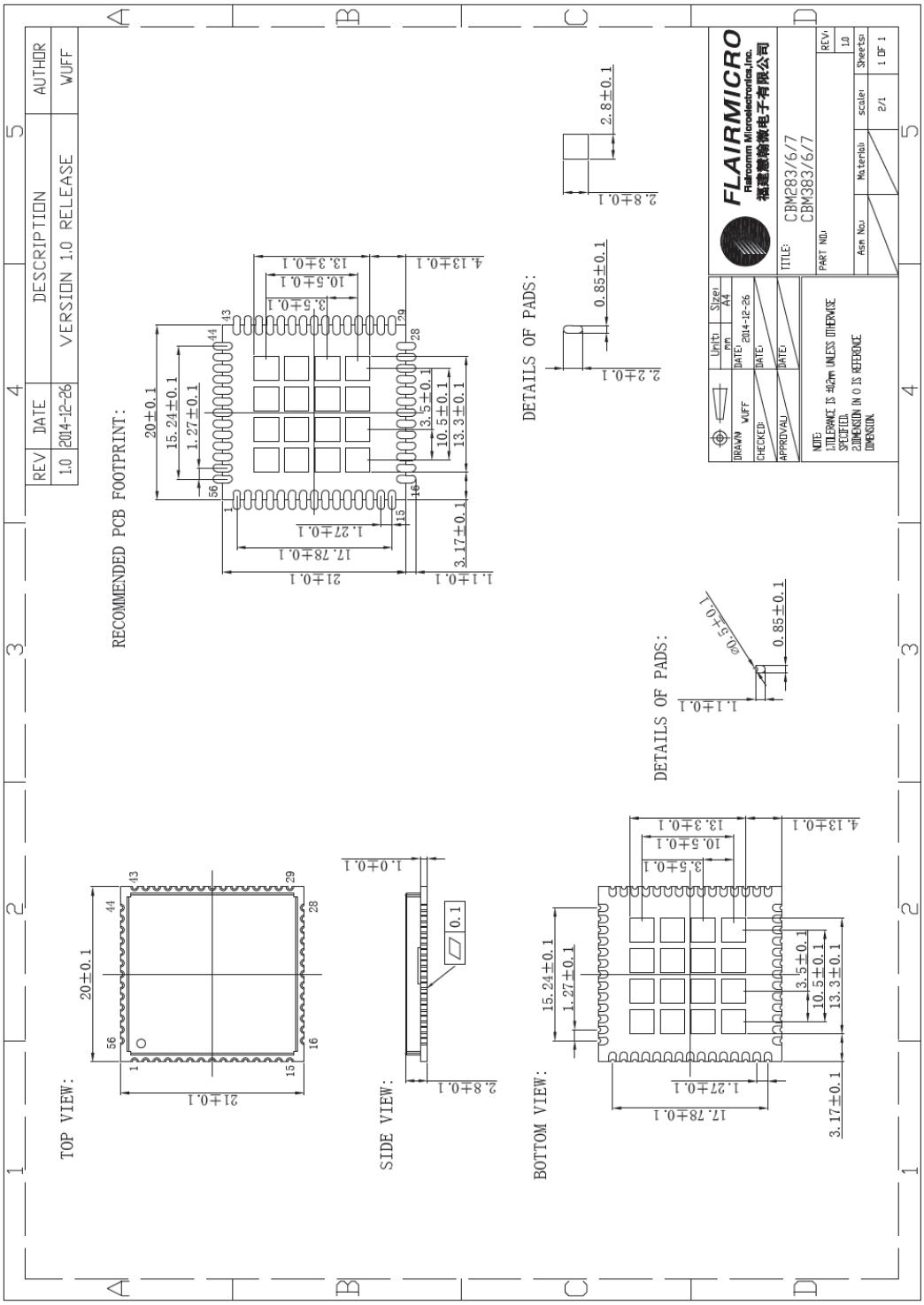

Figure 20: Mechanical Characteristic

10. Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 22** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

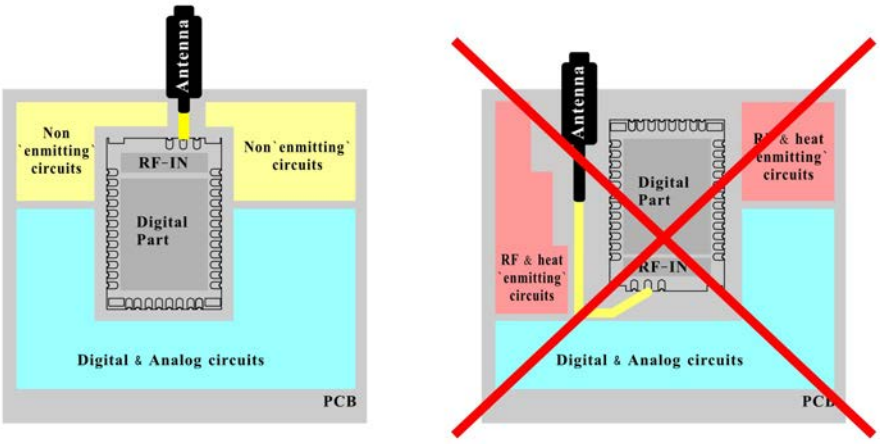

Figure 21: Placement the Module on a System Board

10.1 Antenna Connection and Grounding Plane Design

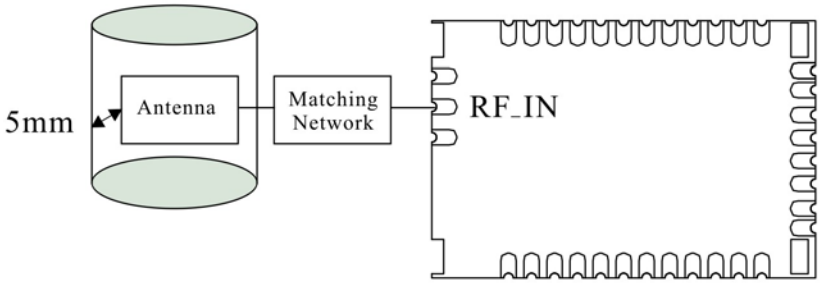

Figure 22: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

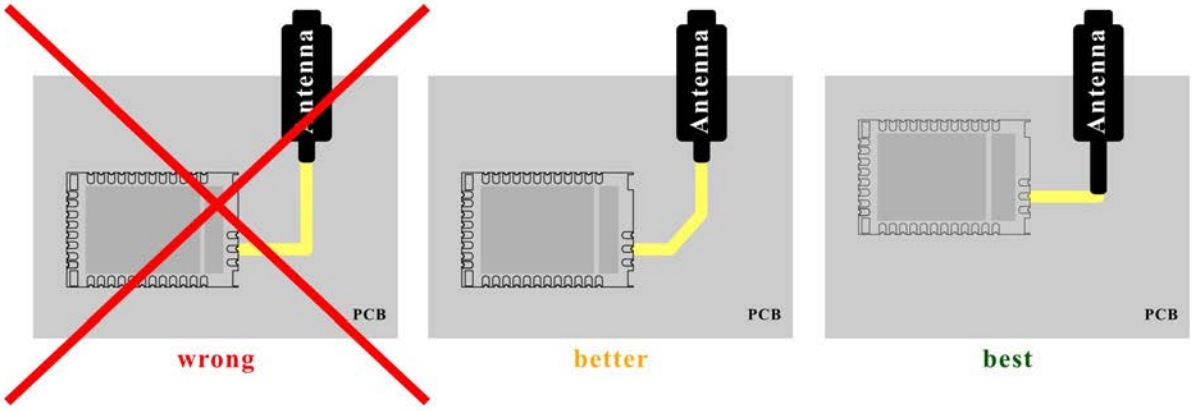

Figure 23: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

11. Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

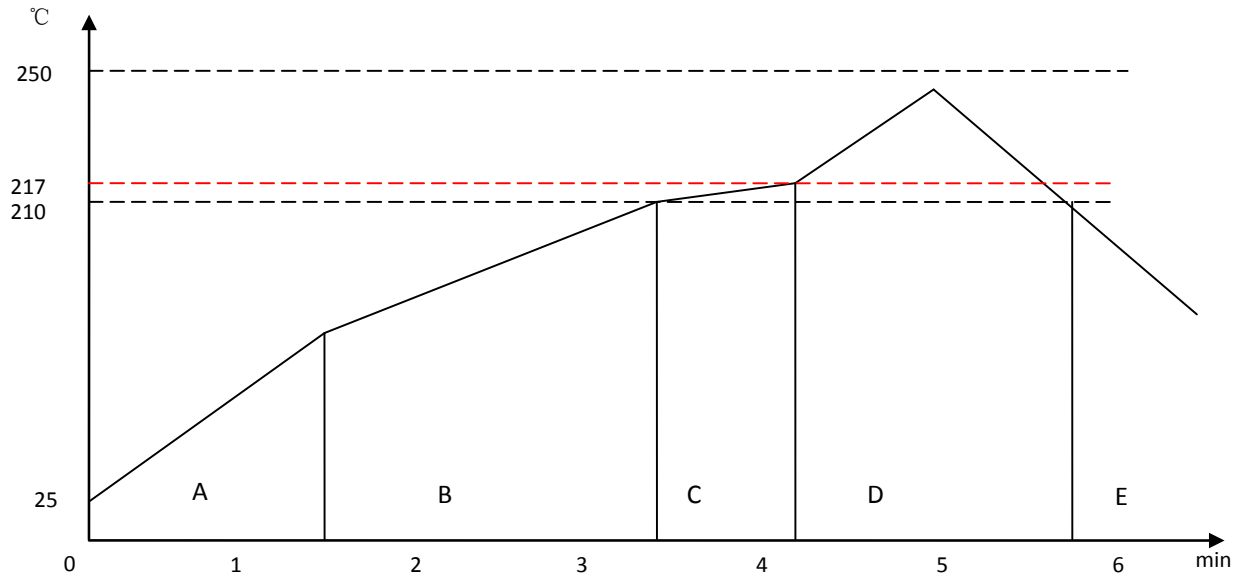

Figure 24: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone**.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C**.

12. Ordering Information

12.1 Product Packaging Information

TBD

Figure 25: Product Packaging Information

12.2 Ordering information

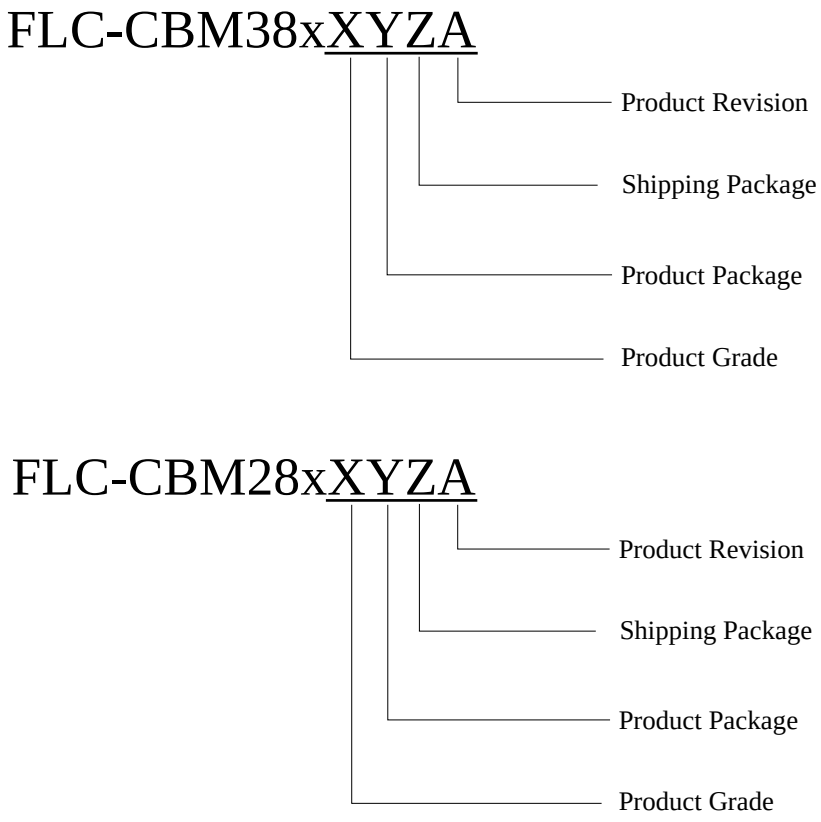

Figure 26: Ordering Information

Package		Order Number
Type	Shipment	CBM38xIQ2A / CBM38xAQ2A CBM28xIQ2A / CBM28xAQ2A
QFN	Tape and reel	

Table 50: Ordering Information

12.2.1 Product Revision

Product Revision	Description	Availability
A	WL/BT Shared Antenna	Yes
B	WL/BT Dual Antenna	Yes

Table 51: Product Revision

12.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	—	No
1	Plastic Tray	800x5 = 4000	No
2	Tape	—	Yes

Table 52: Shipping Package

12.2.3 Product Package

Product Package	Description	Availability
Q	QFN	Yes
L	LGA	No
B	BGA	No
C	Connector	No

Table 53: Product Package

12.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	No
I	Industrial	Yes
V	Automobile After-Market	No
A	Automobile Before-Market	Yes

Table 54: Product Grade