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FLC-CBM251
Datasheet

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Release Record

Version	Release Date	Comments
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TABLES AND FIGURES

1. Introduction

This datasheet describes the FLC-CBM251of multi-function wireless connectivity module. Itis highly integrated module that incorporates WLAN, BTand BLE in a single package. The package is 56 pin 20mmx21mm QFN package. Itprovides a universal platform to meet all wireless connectivity needs in vehicle infotainment device. This device is ideal for addressing all wireless multimedia options within a modern car be it the head unit infotainment console or the rear seat display unit.This module offersautomotive product grade.

- High quality audio based Bluetooth hands-free calling and music
- Multiple Bluetooth connections active simultaneously
- High Definition video sharing between personal portable device and in car infotainment system

1.1 Module Functional Blocks

Product Name	WLAN 2.4GHz	WLAN 5GHz	WLAN 2.4G MIMO	BT, BLE	WL/BT Shared Antenna	WL/BT Dual Antenna	GNSS
CBM251AQ2A	√	√		√	√		

Table 1: Module Functional Blocks

1.2 Block Diagram

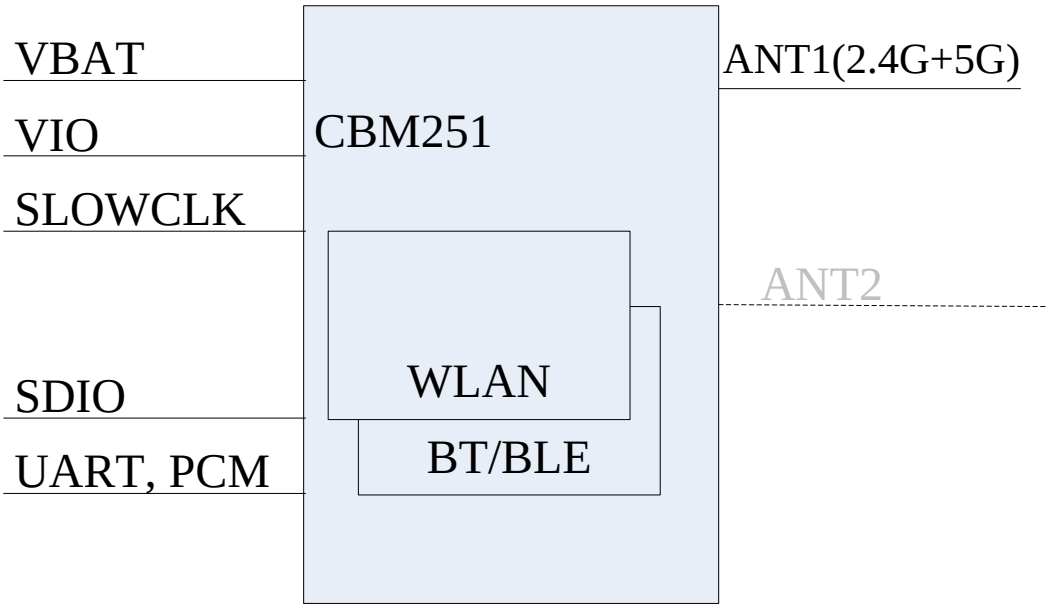


Figure 1：Block Diagram

1.3 Features

- WLAN, BT, BLE on a single packageprovides a unique scalable platform catering to all connectivity needs in vehicle infotainment
- Shared HCI transport for BT/BLE over UART and SDIO for WLAN.
- Supports battery voltage range from 3.0V to 4.8V supplies with internal switching regulator.
- Temperature detection and compensation mechanism ensures minimal variation in RFperformance over the entire temperature range. (-40°C to 85°C)
- BT 4.1, BLE and all audio processing features work in parallel and include full coexistence withWLAN

1.3.1 Bluetooth Features

- Complies with Bluetooth Core Specification Version 4.1 for automotive applications with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM for audio data.

- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Supports low energy host wake-up for long term system sleep capability.

1.3.2 WLAN Features

- IEEE 802.11ac compliant.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Supports RX space-time block coding (STBC)
- Supports IEEE 802.11ac/n beamforming.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Supports standard SDIO v3.0 (including DDR50 mode at 50 MHz and SDR104 mode at 208 MHz, 4-bit and 1-bit), and gSPI (48 MHz) host interfaces.
- Backward compatible with SDIO v2.0 host interfaces.

2. General Specification

Bluetooth	
Standard	Bluetooth 4.1(Dual Mode)
Frequency Band	2.402G ~ 2.480G
RF Input Impedance	50 ohms
Interfaces	UART, PCM/I^2S
WLAN	
Frequency Band	2.4/5.0 GHz
RF Input Impedance	50 ohms
Interfaces	SDIO
RF Input Impedance	50 ohms
Power	
Supply Voltage	3~ 4.8V DC
Typical Working Current	BT:33mA @ DH5 master 3.3V
	WLAN:TBD
Operating Environment	
Temperature	-40ºC to +85ºC
Relative Humidity	Less than 85%
Certifications	TBD
Environmental	RoHS Compliant
Dimension and Weight	
Dimension	21mm(L)*20mm(W)*2.8mm(H)
Weight	2.10~2.25g

Table 2: General Specification

3. Pin Definition

3.1 Pin Configuration

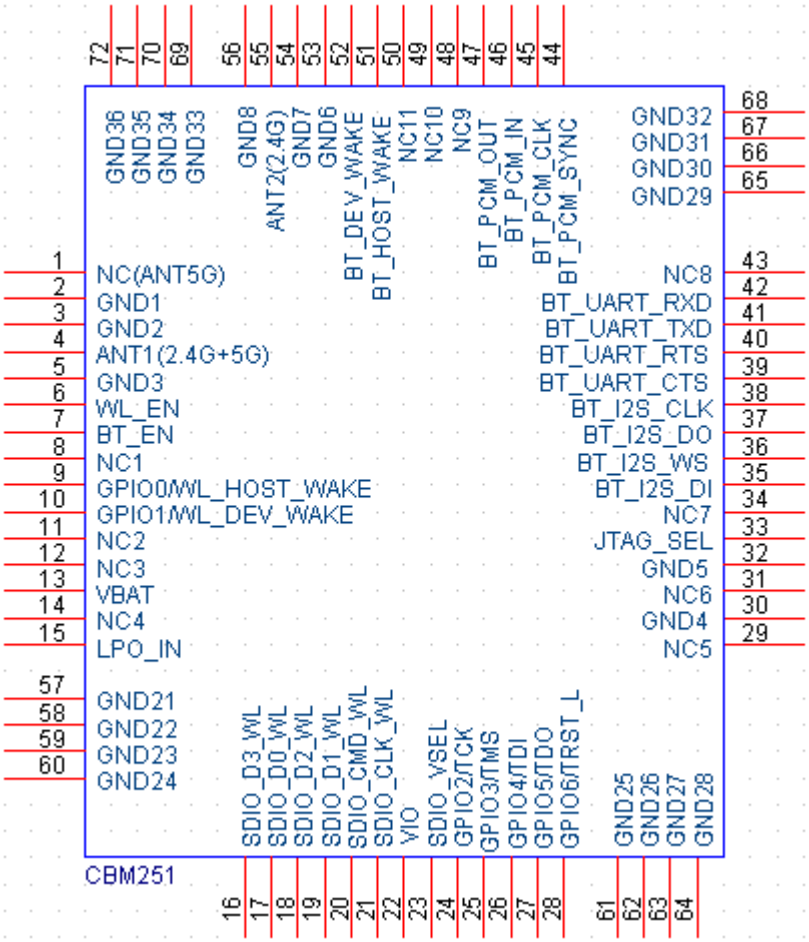


Figure 2: Pin Configuration

3.2 Pin Definition

Pin	Pin Name	I/O Type	Description
1	NC(ANT(5G))	ANA	No Connect.Can be selected by internal for Antenna(5GHz)
2	GND	GND	GND
3	GND	GND	GND
4	ANT1(2.4G+5G)	ANA	Antenna(2.4GHz+5GHz)

5	GND	GND	GND
6	WL_REG_ON	IN	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200kΩ pull- down resistor that is enabled by default. It can be disabled through programming.
7	BT_REG_ON	IN	Used by PMU to power up or power down the internal regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
8	NC		NC
9	GPIO0/WL_HOST_WAKE	I/O	WL_HOST_WAKE
10	GPIO1/WL_DEV_WAKE	I/O	WL_DEV_WAKE
11	NC		NC
12	NC		NC
13	VBAT	POW	Main power supply
14	NC		NC
15	LPO_IN	I	Slow clock. 32.768k
16	SDIO_D3	I/O	SDIO data line 3
17	SDIO_D0	I/O	SDIO data line 0.
18	SDIO_D2	I/O	SDIO data line 2
19	SDIO_D1	I/O	SDIO data line 1
20	SDIO_CMD	I/O	SDIO command line.
21	SDIO_CLK	IN	SDIO clock input.
22	VIO	POW	IO power supply voltage
23	SDIO_VSEL	I/O	Default 0, To change the mode, connect an external PU resistor to VIO , using a 10 kΩ resistor or less
24	GPIO2/TCK	I/O	JTAG TCK is selected when JTAG_SEL pin is high. NC if not used
25	GPIO3/TMS	I/O	JTAG TMS is selected when JTAG_SEL pin is high. NC if not used
26	GPIO4/TDI	I/O	JTAG TDI is selected when JTAG_SEL pin is high. NC if not used
27	GPIO5/TDO	I/O	JTAG TDO is selected when JTAG_SEL pin is high. NC if not used

28	GPIO6/TRST_L	I/O	JTAG TRST_L is selected when JTAG_SEL pin is high. NC if not used
29	NC		NC
30	GND	GND	GND
31	NC		NC
32	GND	GND	GND
33	JTAG_SEL	I/O	JTAG select. Pull high to select the JTAG interface. If the JTAG interface is not used, this pin may be left floating or connected to ground.
34	NC		NC
35	BT_I2S_DI	I/O	I2S data input.
36	BT_I2S_WS	I/O	I2S WS; can be master (output) or slave (input).
37	BT_I2S_DO	I/O	I2S data output.
38	BT_I2S_CLK	I/O	I2S clock, can be master (output) or slave (input).
	BT_UART_CTS	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
40	BT_UART_RTS	O	UART request-to-send. Active- low request-to-send signal for the HCI UART interface. BT LED control pin.
41	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
42	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
43	NC		NC
44	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input).
45	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input).
46	BT_PCM_IN	I	PCM data input.
47	BT_PCM_OUT	O	PCM data output.
48	NC		NC
49	NC		NC
50	NC		NC
51	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE.
52	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE.
53	GND	GND	GND
54	GND	GND	GND
55	NC		NC

56-72	GND	GND	GND

Table 3: Pin Definition

Note:

The Thermal(pin57-pin72) on the Bottom Layer needs to be connected to the GND Layer. Please use as many vias as possible from Top Layer to connect the Thermal to GND Layer.

4. Power Supply and Power Management

4.1 Power Supply

A single VBAT (3.0V to 4.8V DC maximum) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the module. Two control signals, BT_REG_ON and WL_REG_ON, are used to power up the regulators and take the respective section out of reset. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted.

4.2 WLAN Power Management

WLAN power states are described as follows:

- Active mode—All WLAN blocks in the module are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the module remains powered up in an IDLE state. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip, including both analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HWreinitialization.
- Power-down mode—The module is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic reenabling the internal regulators.

4.3 Power-Up Sequence and Timing

It has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.

Description of Control Signals

- WL_REG_ON: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the

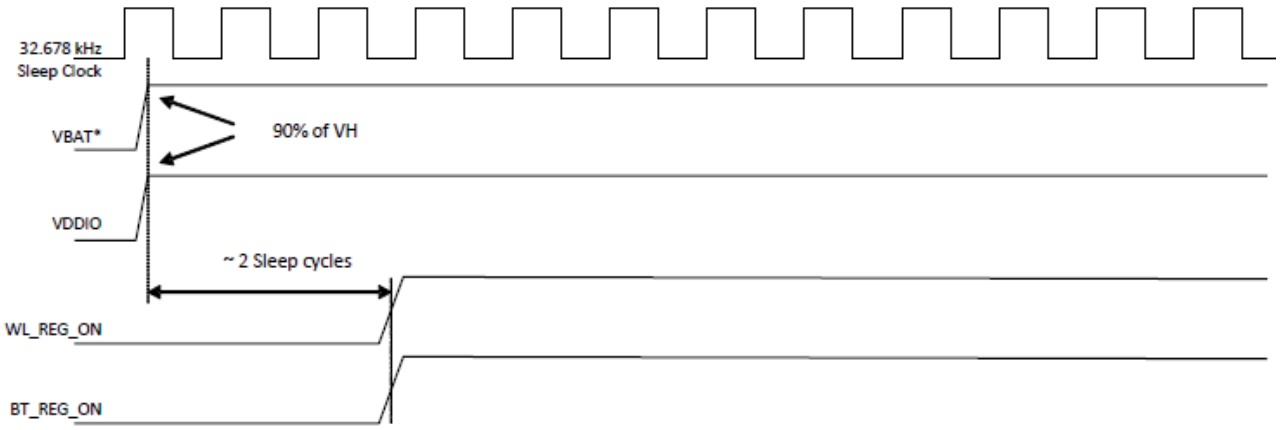
WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

- BT_REG_ON: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

4.3.1 Power-Up States

The correct power-up and shut-down sequences must be followed to avoid damage to the device.

While VBAT or VIO or both are deasserted, no signals should be driven to the device. The only exception is theslow clock that is a fail-safe I/O.

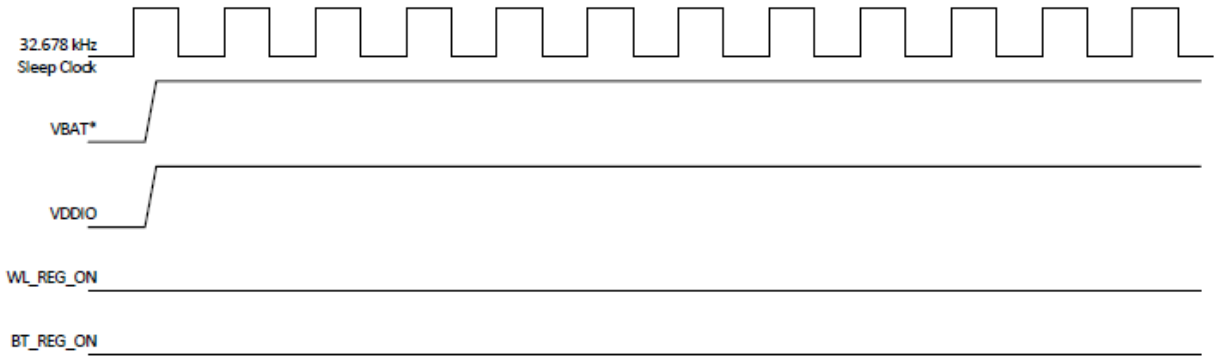


*Notes:

1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.

2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 3: WLAN = ON, Bluetooth = ON

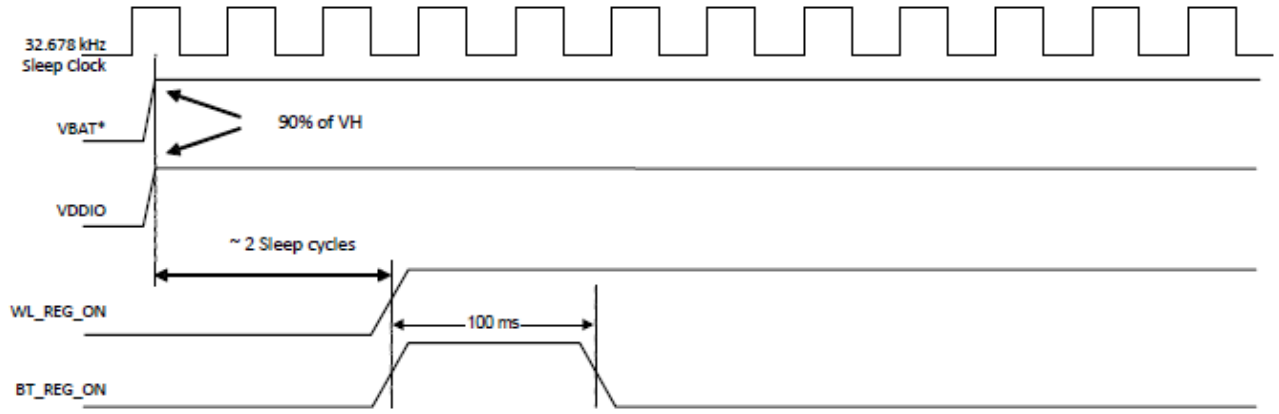


*Notes:

1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.

2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 4:WLAN = OFF, Bluetooth = OFF



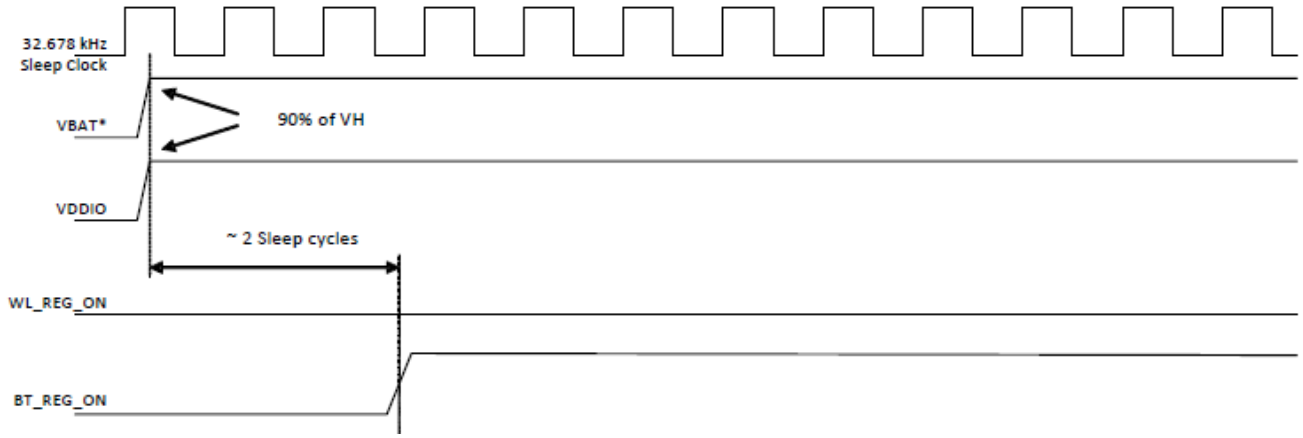
*Notes:

1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.

2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3. Ensure that BT_REG_ON is driven high at the same time as or before WL_REG_ON is driven high. BT_REG_ON can be driven low 100 ms after WL_REG_ON goes high.

Figure 5:WLAN = ON, Bluetooth = OFF



*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high .

Figure 6: WLAN = OFF, Bluetooth = ON

5. Clocks

5.1 Slow Clock / Lpo clock

The slow clock is a free-running clock of 32.768 KHz which is supplied from an external clock source. It is connected to the LPO_IN pin.

Parameter	LPO Clock	Unit
Input slow clock frequency	32768	Hz
Frequency accuracy	±200	ppm
Frequency input duty cycle	30-70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	%
Input impedance	＞100k	Ω
Input capacitance	＜5	pF
Jitter	＜10000	ppm

Table 4: External 32.768 kHz Sleep Clock Specifications

6. Bluetooth Functional Block

6.1 BluetoothSubsystem Overview

The Device is a Bluetooth 4.1 + EDR-compliant, baseband processor/2.4 GHz transceiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth solution.

The Device is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. The Device incorporates all Bluetooth 4.1 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

The Bluetooth radio transceiver provides enhanced radio performance to meet Automotive Grade 3 temperature applications and the tightest integration into automotive platforms. The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability

6.1.1 Features

• Supports key features of upcoming Bluetooth standards

• Fully supports Bluetooth Core Specification version 4.1 + (Enhanced Data Rate) EDR features:

– Adaptive Frequency Hopping (AFH)

– Quality of Service (QoS)

– Extended Synchronous Connections (eSCO)

– Voice Connections – Fast Connect (interlaced page and inquiry scans)

– Secure Simple Pairing (SSP) – Sniff Subrating (SSR)

– Encryption Pause Resume (EPR)

– Extended Inquiry Response (EIR)

– Link Supervision Timeout (LST)

• UART baud rates up to 4 Mbps

• Supports Bluetooth 4.1 for automotive applications

• Supports maximum Bluetooth data rates over HCI UART

• Multipoint operation with up to seven active slaves

– Maximum of seven simultaneous active ACL links

– Maximum of three simultaneous active SCO and eSCO connections with scatternet support

• Trigger Broadcom fast connect (TBFC)

• Narrowband and wideband packet loss concealment

• Scatternet operation with up to four active piconets with background scan and support for scatter mode
• High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling
• Channel quality driven data rate and packet type selection
• Standard Bluetooth test modes
• Extended radio and production test mode features
• Full support for power savings modes
  – Bluetooth clock request
  – Bluetooth standard sniff
  – Deep-sleep modes and software regulator shutdown

6.1.2 Blue Radio

The Devicehas an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality.

6.1.2.1 Transmitter

The module features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path performs signal filtering, I/Q upconversion, output power amplification, and RF filtering. The transmitter path also incorporates /4-DQPSK and 8-DPSK modulations for 2Mbps and 3Mbps EDR support, respectively. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth Class 1 or Class 2 operation.

6.1.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, /4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

6.1.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

6.1.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated telematics applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near-thermal-noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength

indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

6.1.2.5 Receive

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the module to be used in most applications with minimal off-chip filtering. For integrated telematics operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

6.1.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

6.2 Bluetooth Baseband Core BT Receiver

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data:

• Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.

• Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

6.2.1 Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features, with the following benefits:

• Dual-mode Bluetooth Low Energy (BT and BLE operation)

• Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.

• Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.

• Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.

• Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.

• Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.

• QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

6.2.2 Bluetooth Low Energy

The Device supports the Bluetooth Low Energy operating mode

6.2.3 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

• Major states:
  – Standby
  – Connection
• Substates:
  – Page
  – Page Scan
  – Inquiry
  – Inquiry Scan – Sniff

6.2.4 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core.

6.2.4.1 RF Power Management

The BBC generates power-down control signals to the 2.4 GHz transceiver for the transmit path, receive path, PLL, and power amplifier. The transceiver then processes the power-down functions accordingly.

6.2.4.2 Host Controller Power Management

When running in UART mode, the module may be configured so that dedicated signals are used for power management handshaking between the module and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

signal	type	description
BT_DEV_WAKE	I	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: The Bluetooth device must wake-up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low
BT_HOST_WAKE	0	Host wake up. Signal from the module to the host indicating that the module requires attention. • Asserted: host device must wake-up or remain awake. • Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

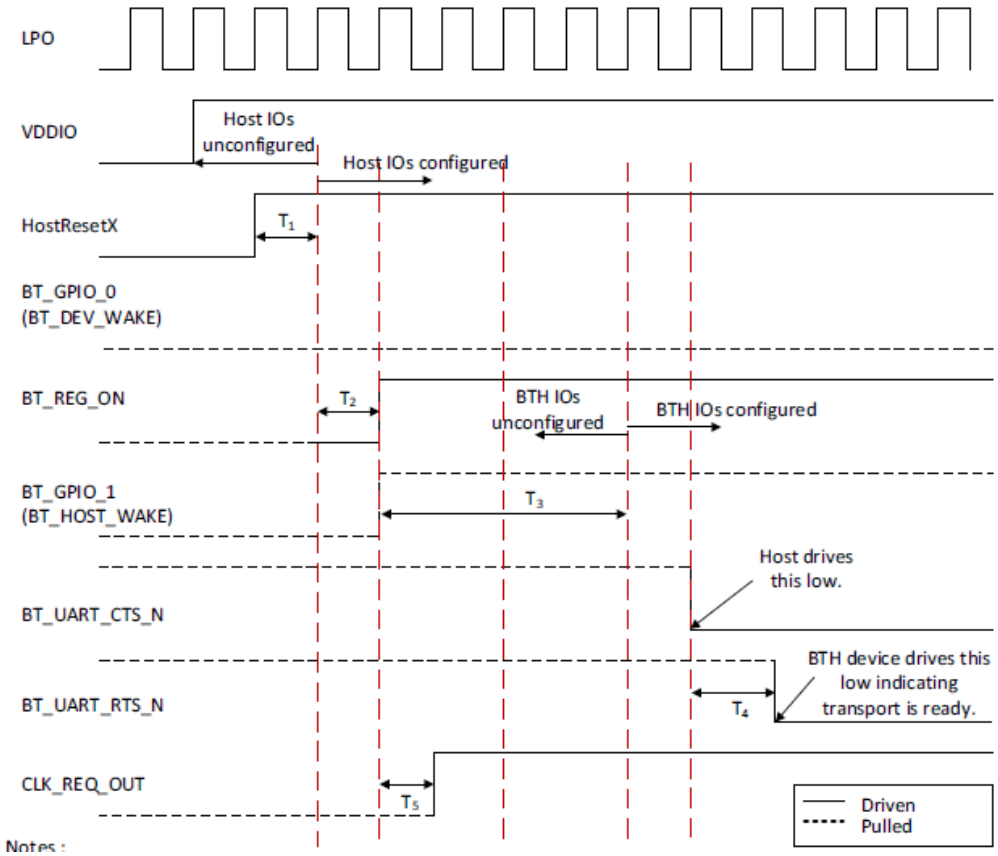


Figure 7:Startup Signaling Sequence

Notes :
1.T1 is the time for the host to settle its IOs after a reset.
2.T2 is the time for the host to drive BT_REG_ON high after the host IOs are configured.
3.T3 is the time for the BTH device to settle its IOs after a reset and the reference clock settling time has elapsed.
4.T4 is the time for the BTH device to drive BT_UART_RTS_N low after the host drives BT_UART_CTS_N low. This assumes the BTH device has completed initialization.

5.T5 is the time for the BTH device to drive CLK_REQ_OUT high after BT_REG_ON goes high. The CLK_REQ_OUT pin is used in designs that have an external reference clock source from the host. It is irrelevant on clock-based designs where the BTH device generates its own reference clock from an external crystal connected to its oscillator circuit.
6.The timing diagram assumes that VBAT is present.

6.2.4.3 BBC Power Management

The following are low-power operations for the BBC:

• Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.

• Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the module runs on the low-power oscillator and wakes up after a predefined time period.

• A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the module is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the module to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O. During the low-power shut-down state, provided VIO remains applied to the module, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the module to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

6.2.4.4 Wideband Speech

The device provides support for wideband speech (WBS) using on-chip SmartAudio technology. The device can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

6.2.4.5 Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bitstream. Packet loss can be mitigated in several ways:

• Fill in zeros.

• Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).

• Repeat the last frame (or packet) of the received bitstream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The module uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality.

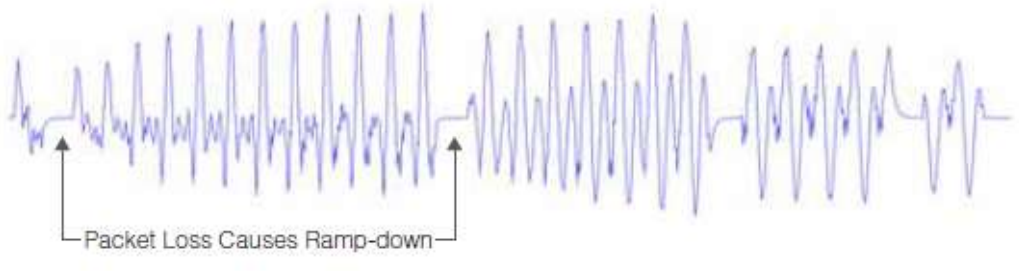


Figure 8:CVSD Decoder Output Waveform Without PLC

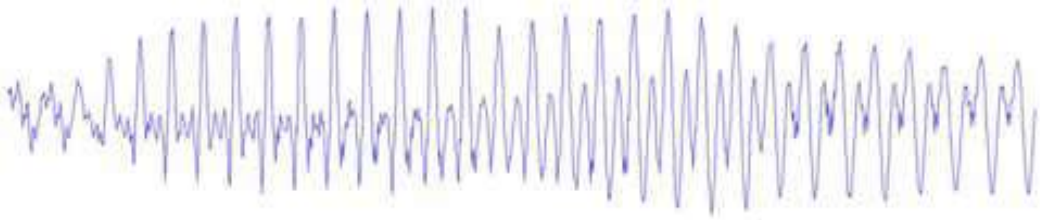


Figure 9:CVSD Decoder Output Waveform After Applying PLC

6.2.4.6 Audio Rate-Matching Algorithms

The device has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth audio data rates.

6.2.4.7 Codec Encoding

The device can support SBC and mSBC encoding and decoding for wideband speech.

6.2.4.8 Multiple Simultaneous A2DP Audio Streams

The device has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

6.2.5 Adaptive Frequency Hopping

The module gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

6.2.6 Advanced Bluetooth/WLAN Coexistence

The device includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as infotainment and telematics modules, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo. Support is provided for platforms that share a single antenna between Bluetooth and WLAN. The module radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution

(shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception. The device integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement. The device also supports Transmit Power Control (TPC) on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non- WLAN 2.4 GHz interference). The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

6.2.7 Fast Connection

The device supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6.3 Microprocessor and Memory Unit for Bluetooth

6.3.1 Overview

The Bluetooth microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI). The ARM core is paired with a memory unit that contains 608KB of ROM memory for program storage and boot ROM, 192KB of RAM for data scratch-pad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory. External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or feature additions. These patches may be downloaded from the host to the device through the UART transports.

6.3.2 Reset

The device has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes high. If BT_REG_ON is low, then the POR circuit is held in reset.

6.4 Bluetooth Peripheral Transport Unit

6.4.1 PCMInterrface

The device supports two independent PCM interfaces that share pins with the I2S interfaces. The PCM Interface on the device can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are

inputs to the device. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

6.4.1.1 Slot Mapping

The device supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

6.4.1.2 Frame Synchronization

The device supports both short- and long-frame synchronization in both master and slave modes. In short- frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

6.4.1.3 Data Formatting

The device may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

6.4.1.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The device also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

6.4.1.5 Multiplexed Bluetooth Over PCM

To support multiple Bluetooth audio streams within the Bluetooth channel, both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. Figure 10 shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the

transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

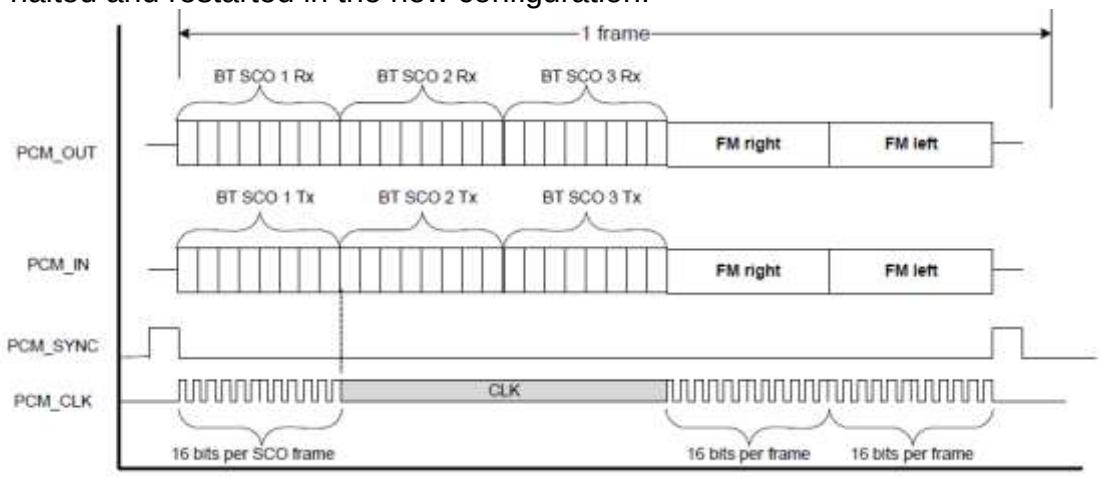


Figure 10:Functional Multiplex Data Diagram

Each SCO channel duplicates the data 6 times. Each WBS frame duplicates the data 3 times per frame

6.4.1.6 PCM Interface Timing

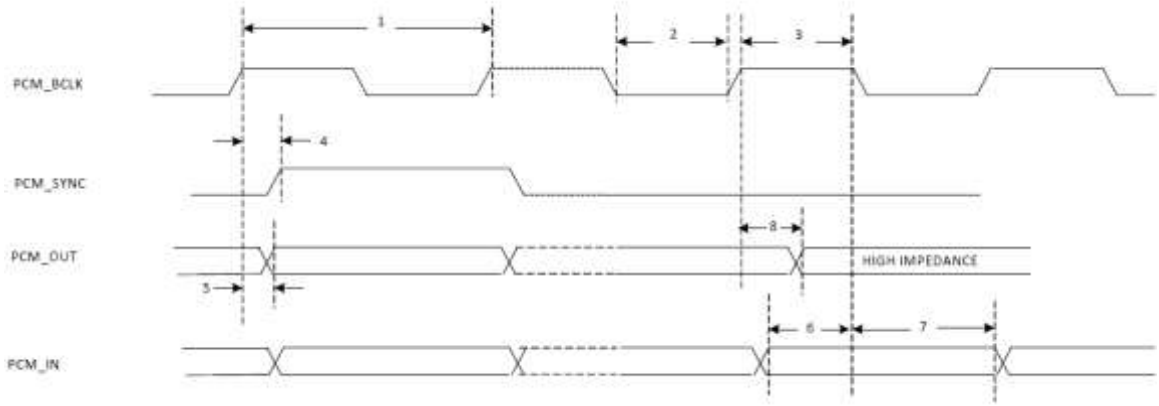


Figure 11: PCM Timing Diagram (Short Frame Sync, Master Mode)

RefN	Characteristics	Minimum	Typical	Maximum	Unit
1	PCMbitclockfrequency	–	–	12	MHz
2	PCMbitclockLOW	41	–	–	ns
3	PCMbitclockHIGH	41	–	–	ns
4	PCM_SYNCdelay	0	–	25	ns
5	PCM_OUTdelay	0	–	25	ns
6	PCM_INsetup	8	–	–	ns
7	PCM_INhold	8	–	–	ns
8	DelayfromrisingedgeofPCM_BCLKduringlastbit periodtoPCM_OUTbecominghighimpedance	0	–	25	ns

Table 5: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

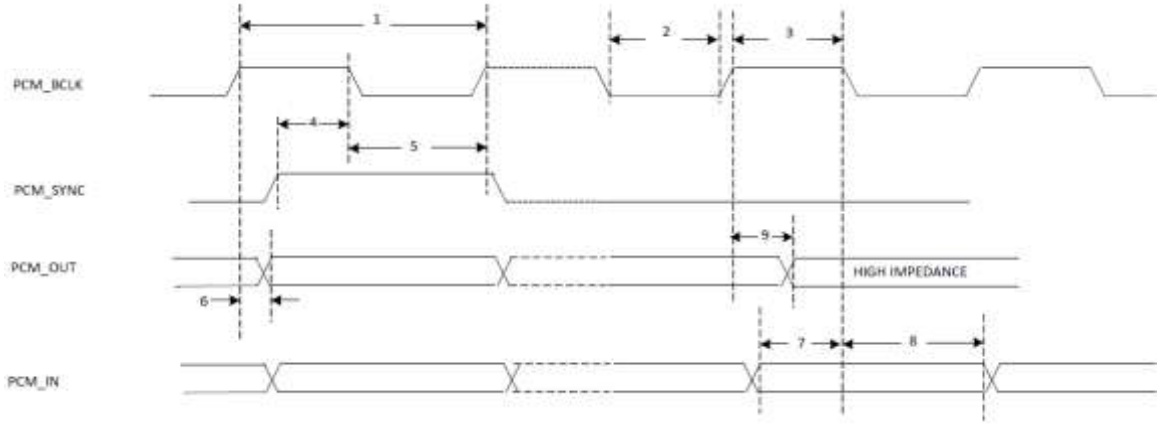


Figure 12:PCM Timing Diagram (Short Frame Sync, Slave Mode)

RefN	Characteristics	Minimum	Typical	Maximum	Unit
1	PCMbitclockfrequency	–	–	12	MHz
2	PCMbitclockLOW	41	–	–	ns
3	PCMbitclockHIGH	41	–	–	ns
4	PCM_SYNCsetup	8	–	–	ns
5	PCM_SYNChold	8	–	–	ns
6	PCM_OUTdelay	0	–	25	ns
7	PCM_INsetup	8	–	–	ns
8	PCM_INhold	8	–	–	ns
9	Delayfromrisingedgeof PCM_BCLKduringlastbit periodto PCM_OUTbecominghighimpedance	0	–	25	ns

Table 6: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

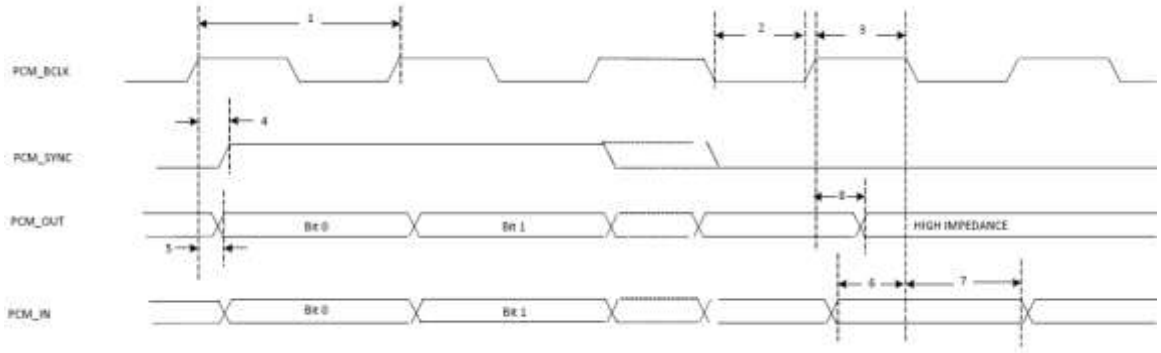


Figure 13:PCM Timing Diagram (Long Frame Sync, Master Mode)

RefN	Characteristics	Minimum	Typical	Maximum	Unit
1	PCMbitclockfrequency	–	–	12	MHz
2	PCMbitclockLOW	41	–	–	ns

3	PCMbitclockHIGH	41	–	–	ns
4	PCM_SYNCdelay	0	–	25	ns
5	PCM_OUTdelay	0	–	25	ns
6	PCM_INsetup	8	–	–	ns
7	PCM_INhold	8	–	–	ns
8	Delayfromrisingedgeof PCM_BCLKduringlastbit periodto PCM_OUTbecominghighimpedance	0	–	25	ns

Table 7: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

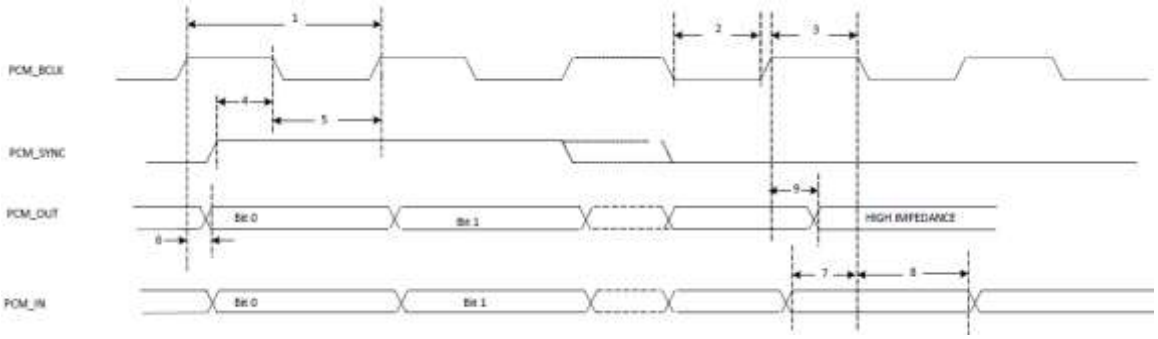


Figure 14: PCM Timing Diagram (Long Frame Sync, Slave Mode)

RefN	Characteristics	Minimum	Typical	Maximum	Unit
1	PCMbitclockfrequency	–	–	12	MHz
2	PCMbitclockLOW	41	–	–	ns
3	PCMbitclockHIGH	41	–	–	ns
4	PCM_SYNCsetup	8	–	–	ns
5	PCM_SYNChold	8	–	–	ns
6	PCM_OUTdelay	0	–	25	ns
7	PCM_INsetup	8	–	–	ns
8	PCM_INhold	8	–	–	ns
9	Delayfromrisingedgeof PCM_BCLKduringlastbit periodto PCM_OUTbecominghighimpedance	0	–	25	ns

Table 8:PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

6.4.2 Uart Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command. UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud. The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The device UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state. Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The device UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

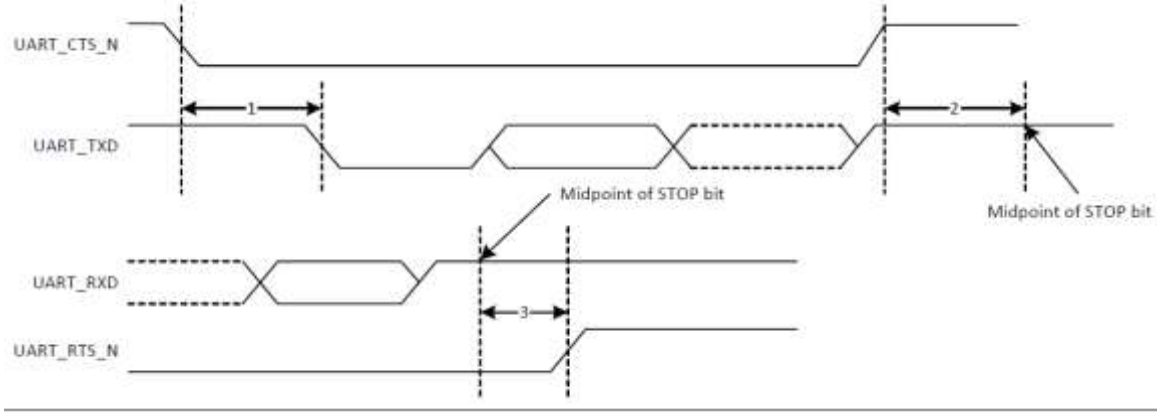


Figure 15:UART Timing

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delaytime,UART_CTS_NlowtoUART_TXDvalid	–	–	1.5	Bitperiod
2	Setuptime,UART_CTS_Nhighbeforemidpointofstopbit	–	–	0.5	Bitperiod
3	Delaytime,midpointof stopbitto UART_RTS_Nhigh	–	–	0.5	Bitperiod

Table 9:UART Timing Specifications

6.4.3 I2S Interface

The device supports two independent I2S digital audio ports. The I2S signals are:

- I2S clock: I2S SCK
- I2S Word Select: I2S WS
- I2S Data Out: I2S SDO
- I2S Data In: I2S SDI

I2S SCK and I2S WS become outputs in master mode and inputs in slave mode, while I2S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I2S bus, per the I2S specification. The MSB of each data word is transmitted one bit clock cycle after the I2S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I2S WS is low, and right-channel data is transmitted when I2S WS is high. Data bits sent by the device are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32bits per frame = 1.536MHz

48 kHz x 50bits per frame = 2.400MHz
The master clock is generated from the input reference clock using a N/M clock divider.
In the slave mode, any clock rate is supported to a maximum of 3.072MHz

6.4.3.1 I2S Timing

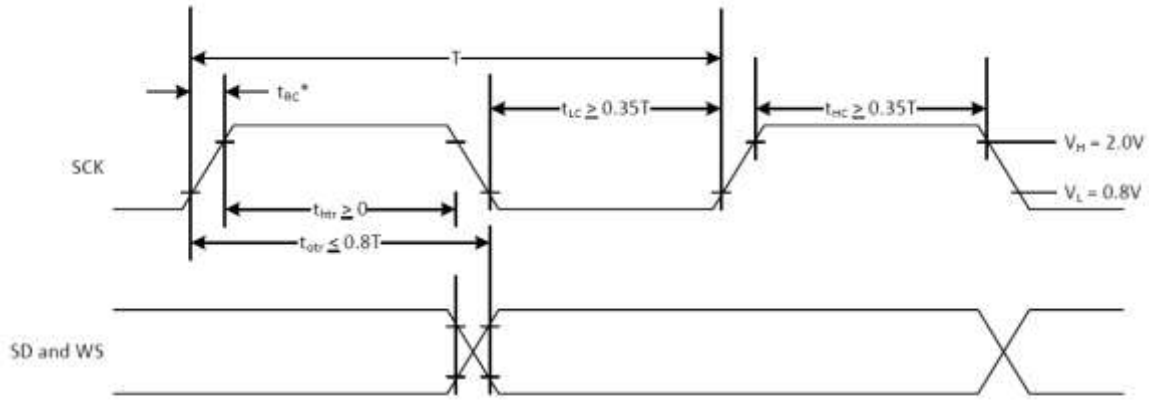
Note: Timing values specified in Table11 are relative to high and low threshold levels.

	Transmitter				Receiver				
	LowerLImit		UpperLimit		LowerLimit		UpperLimit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max	Notes
ClockPeriodT	T_{tr}	–	–	–	T_r	–	–	–	a
MasterMode:Clockgeneratedby transmitterorreceiver									
$HIGHt_{HC}$	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
$LOWt_{LC}$	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
SlaveMode:Clockacceptedby transmitterorreceiver									
$HIGHt_{HC}$	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
$LOWt_{LC}$	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
$Risetimet_{RC}$	–	–	$0.15T_{tr}$	–	–	–		–	d
Transmitter									
$Delayt_{dtr}$	–	–	–	0.8T	–	–	–	–	e
$Holdtimet_{htr}$	0	–	–	–	–	–	–	–	d
Receiver									
$Setuptimet_{sr}$	–	–	–	–	–	$0.2T_r$	–	–	f
$Holdtimet_{hr}$	–	–	–	–	–	0	–	–	f

Table 10: Timing for I2S Transmitters and Receivers

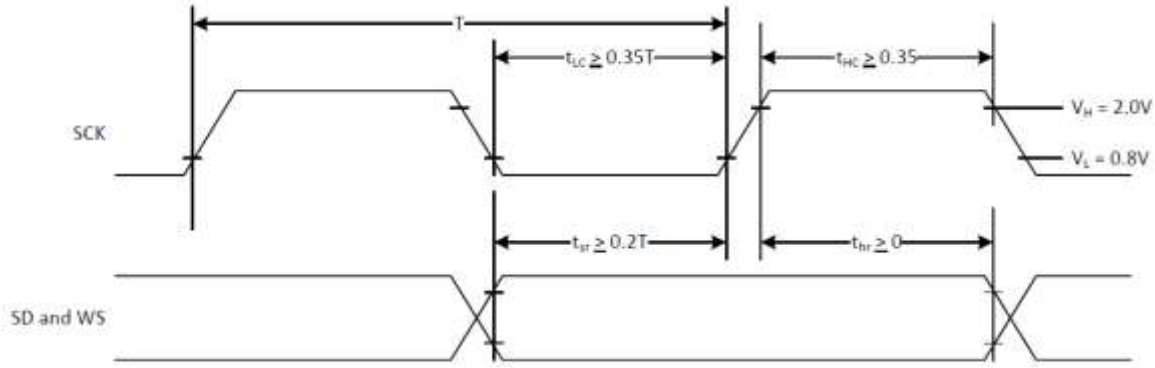
a.The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver have to be able to handle the data transfer rate.
b.At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.
c.In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.
d.Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter has to guarantee that thtr is greater than or equal to zero, so long as the clock rise-time tRC is not more than tRCmax, where tRCmax is not less than 0.15Ttr
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

Note: The time periods specified in Figure15 and Figure16 are defined by the transmitter speed. The receiver specifications must match transmitter performance.



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 16: I2S Transmitter Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Figure 17: I2S Receiver Timing

7. WLAN Functional Block

7.1 WLAN Global Function

7.1.1 WLAN CPU and Memory Subsystem

The device WLAN section includes an integrated ARM Cortex-R4™ 32-bit processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features low gate count, low interrupt latency, and low- cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering more than 30% performance gain over ARM7TDMI, the ARM Cortex-R4 implements the ARM v7-R architecture with support for the Thumb®-2 instruction set. At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes. Using multiple technologies to reduce cost, the ARM Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and System buses), and extensive debug features including real time trace of program execution. On-chip memory for the CPU includes 768 KB SRAM and 640 KB ROM.

7.1.2 GPIO Interface

The following number of general-purpose I/O (GPIO) pins are available on the WLAN section of the device that can be used to connect to various external devices:

• 0 – 6 GPIO

Upon power up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions

GPIO_0	WL_HOST_WAKE
GPIO_1	WL_DEV_WAKE
GPIO_2	TCK, GCI_GPIO_1, or UART RX
GPIO_3	TMS or GCI_GPIO_0
GPIO_4	TDI or SECI_IN
GPIO_5	TDO or SECI_OUT
GPIO_6	TRST_L or UART TX

7.1.3 UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins .Provided primarily for debugging during development, this UART enables the device to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with

other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

7.2 WLAN Host Interface

7.2.1 SDIO v3.0

The device WLAN section supports SDIO version 3.0, including the new UHS-I modes:
• DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
• HS: High speed up to 50 MHz (3.3V signaling).
• SDR12: SDR up to 25 MHz (1.8V signaling).
• SDR25: SDR up to 50 MHz (1.8V signaling).
• SDR50: SDR up to 100 MHz (1.8V signaling).
• SDR104: SDR up to 208 MHz (1.8V signaling).
• DDR50: DDR up to 50 MHz (1.8V signaling).
Note: The device is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

The following three functions are supported:
• Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)
• Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max. BlockSize/ByteCount = 64B)
• Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max. BlockSize/ByteCount = 512B)

SD4-BitMode		SD1-BitMode		gSPIMode	
DATA0	Dataline0	DATA	Dataline	DO	Dataoutput
DATA1	Dataline1orInterrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Dataline2orReadWait	RW	ReadWait	NC	Notused
DATA3	Dataline3	N/C	Notused	CS	Cardselect
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Commandline	CMD	Commandline	DI	Datainput

Table 11: SDIO Pin Description

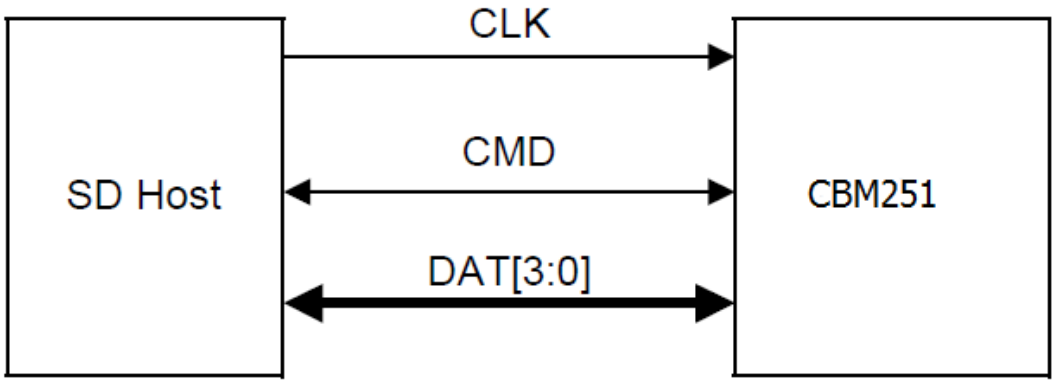


Figure 18:Signal Connections to SDIO Host (SD 4-Bit Mode)

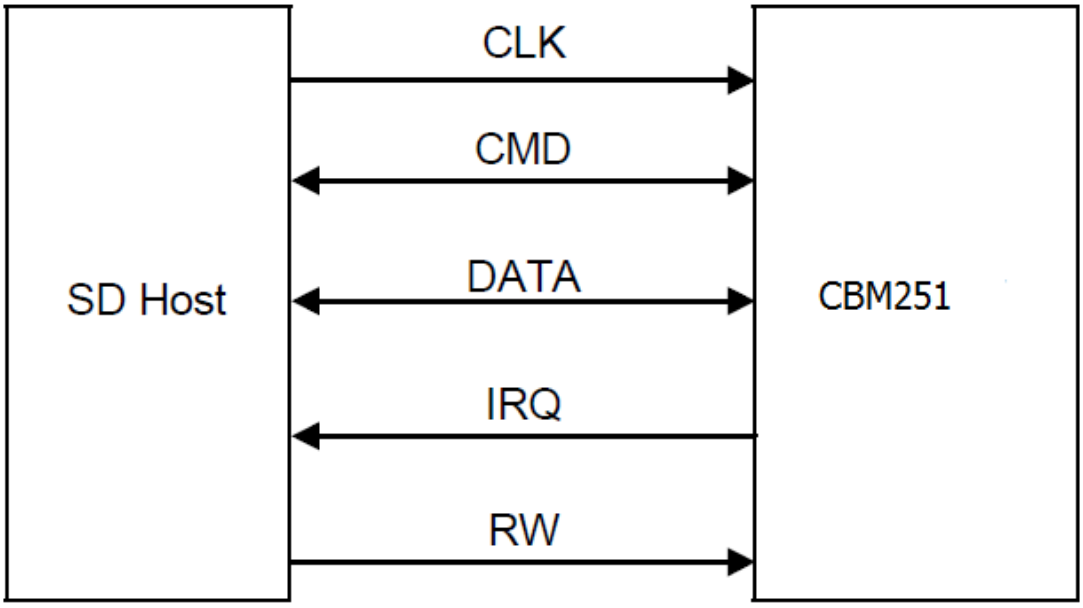


Figure 19: Signal Connections to SDIO Host (SD 1-Bit Mode)

Note: Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

7.2.2 Generic SPI Mode

In addition to the full SDIO mode, the device includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Supports up to 48 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host gSPI frames (16 or 32 bits)
- Supports up to 2 KB frame size per transfer
- Supports little endian (default) and big endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

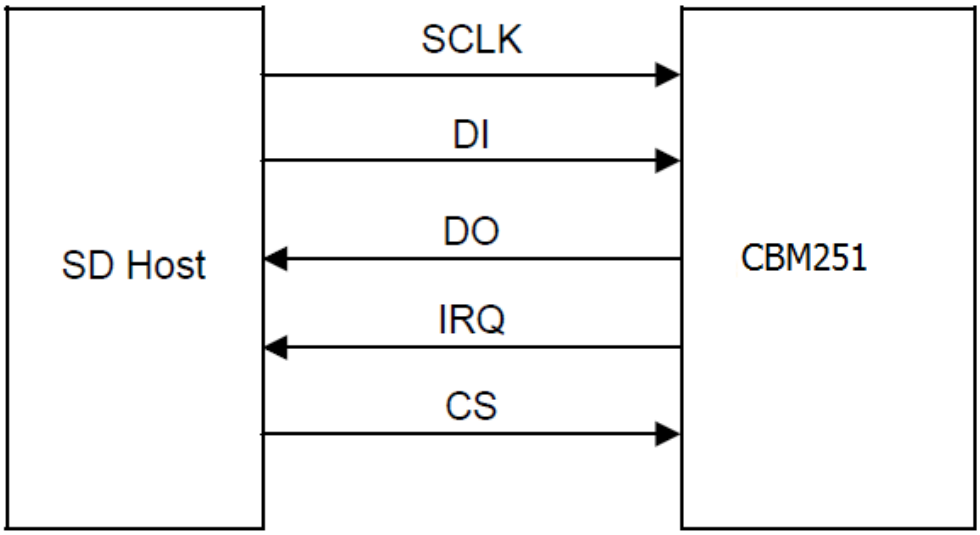


Figure 20:Signal Connections to SDIO Host (gSPI Mode)

7.2.3 Boot-Up Sequence

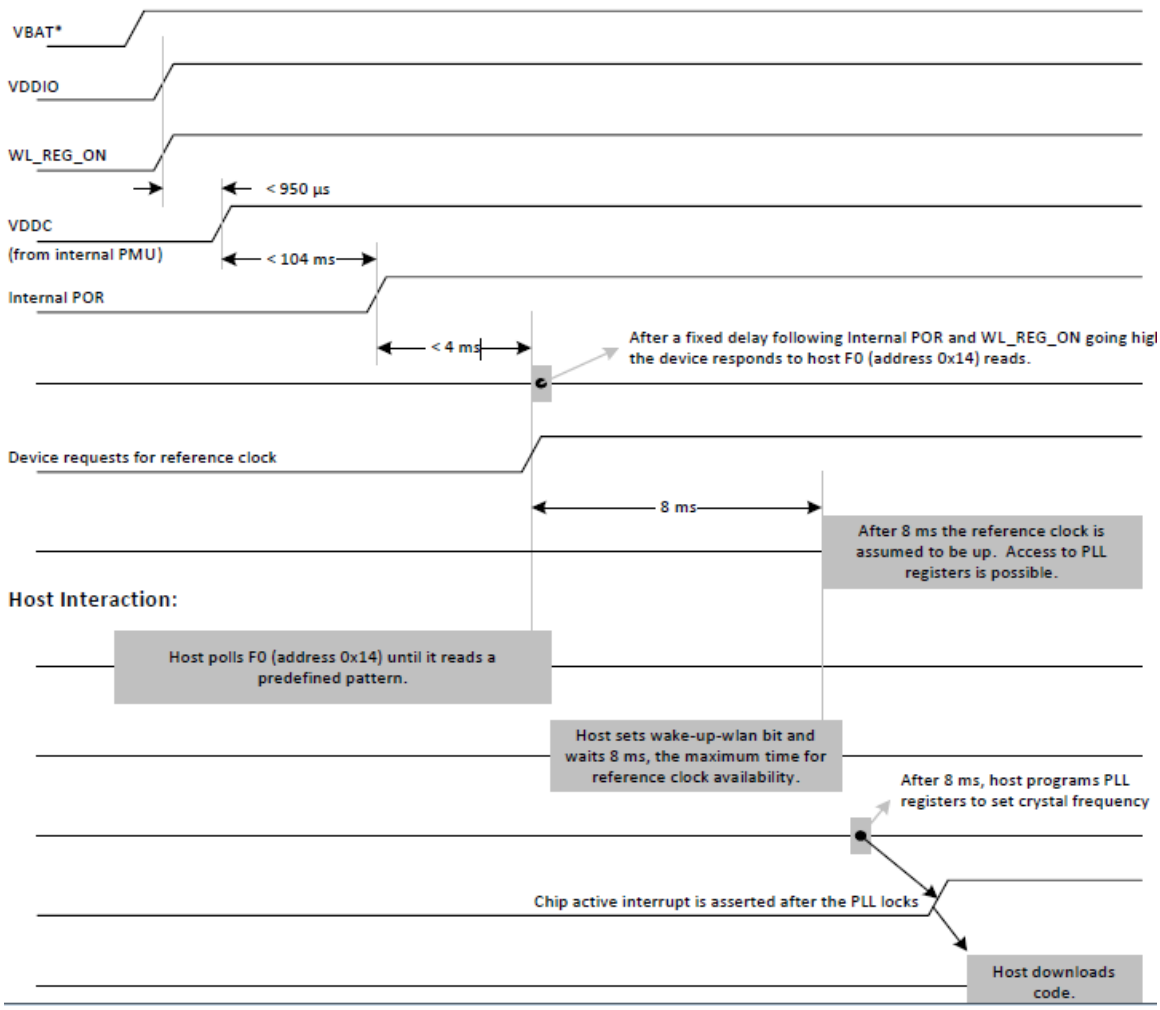


Figure 21: WLAN Boot-Up Sequence

7.3 Wireless LAN MAC and PHY

7.3.1 IEEE 802.11ac MAC

The device WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization.

The following sections provide an overview of the important modules in the MAC

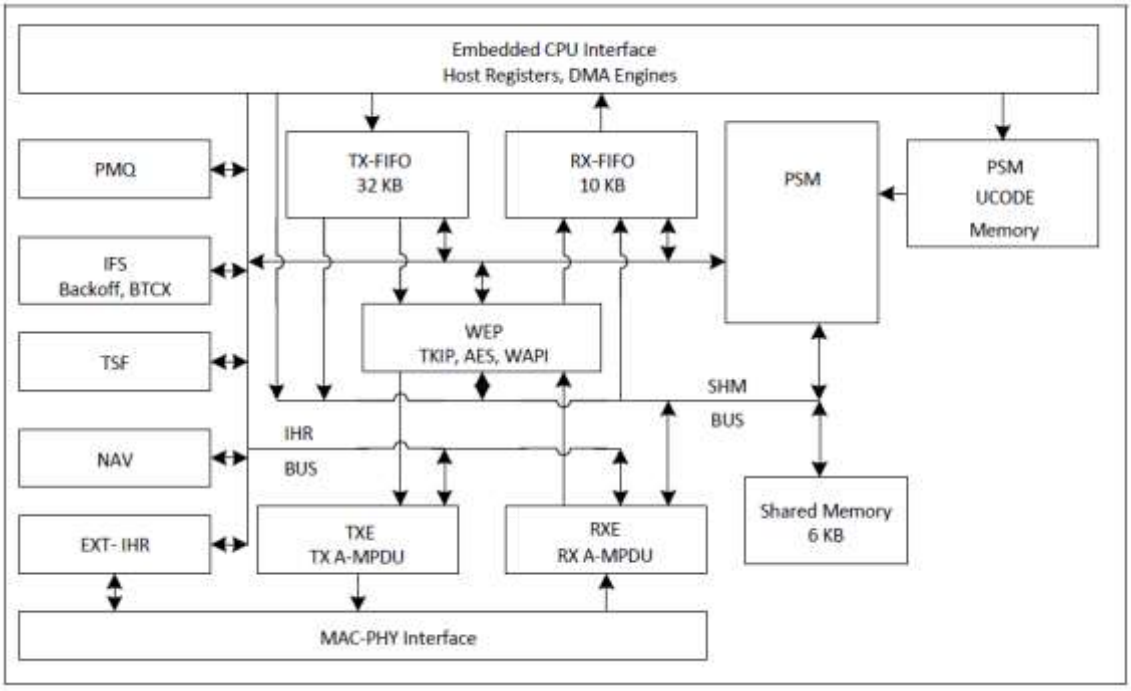


Figure 22: WLAN MAC Architecture

The device WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:
• Enhanced MAC for supporting IEEE 802.11ac features
• Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
• Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
• Support for immediate ACK and Block-ACK policies
• Interframe space timing support, including RIFS
• Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges • Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
• Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
• Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
• Support for coexistence with Bluetooth and other external radios
• Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
• Statistics counters for MIB support

7.3.1.1 PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations

are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch-pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch- pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

7.3.1.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

7.3.1.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

7.3.1.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.
The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.
The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

7.3.1.5 IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.
The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).
The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.
The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.
The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

7.3.1.6 TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.
The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

7.3.1.7 NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier- sense indication.

7.3.1.8 MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

7.3.2 IEEE 802.11ac PHY

The device WLAN Digital PHY is designed to comply with IEEE 802.11ac and IEEE 802.11a/b/g/n single- stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 433.3 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous RX-RX.

The key PHY features include:

• Programmable data rates from MCS0–9 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac

• Supports Optional Short GI mode in TX and RX

• TX and RX LDPC for improved range and power efficiency

• Supports optional space-time block code (STBC) receive of two space-time streams for improved throughput and range in fading channel environments.

• All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.

• Supports IEEE 802.11h/k for worldwide operation

• Advanced algorithms for low power, enhanced sensitivity, range, and reliability

• Algorithms to improve performance in presence of Bluetooth

• Automatic gain control scheme for blocking and non blocking application scenario for cellular applications

• Closed loop transmit power control

• Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities

• On-the-fly channel frequency and transmit power selection

• Supports per packet RX antenna diversity
• Available per-packet channel quality and signal strength measurements
• Designed to meet FCC and other worldwide regulatory requirements

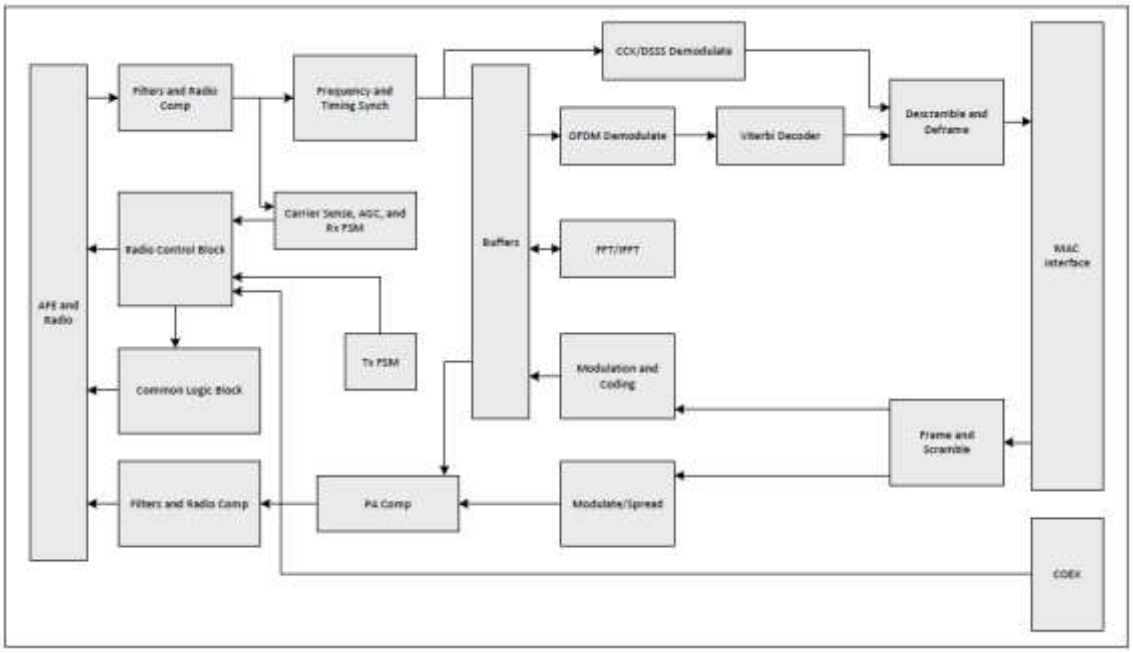


Figure 23: WLAN PHY Block Diagram

7.4 WLAN Radio Subsystem

The device includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

7.4.1 Receiver Path

The device has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN receivers, while the 5 GHz receive path has a dedicated on-chip LNA.

7.4.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications. closed-loop output power control is completely integrated.

8. DC Characteristics

8.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.5	6	V
VIO	-0.5	3.9	V
Maximum undershoot voltage for I/O		-0.5	V
Maximum overshoot voltage for I/O		VIO + 0.5	V

Table 12: Absolute Maximum Rating

1) The absolute maximum ratings in Table 12 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

2) The maximum continuous voltage is 4.8V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.0V (for up to 250 seconds), cumulative duration over the lifetime of the device, are allowed.

3) Duration not to exceed 25% of the duty cycle.

8.2 Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
OperationTemperature (T_A)	–40 to +85	°C	–
StorageTemperature	–40 to +85	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Table 13: Environmental Ratings

8.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

PinType	Symbol	Condition	ESDRating	Unit
ESD,Handling Reference: NQY00083,Section 3.4,GroupD9,Table B	ESD_HAND_HBM	Humanbody model: AEC-Q100-002 REV-E	±1000	V
CDM	ESD_HAND_CDM	Chargeddevicemodel: AEC-Q100-011 REV-C1	±150 (WLANpins)±250 (non-WLAN pins)	V
MM	ESD_MM	8.3.1.1.1 Mach inemodel: 8.3.1.1.2 AEC-	±30	V

Table 14: ESD Specifications

8.4 Recommended Operating Conditions and DC Characteristics

Parameter	Condition	Sym	Min	Max	Unit
VBAT	DC supply voltage for VBAT		3	4.8	V
VIO	DC supply voltage for I/O		1.71	3.63	
For VIO=1.8V;SDIO Interface I/O Pins					
Input high voltage		VIH	1.27		
Input low voltage		VIL		0.58	
Output high voltage	@ 2 mA	VOH	1.4		
Output low voltage	@ 2 mA	VOL		0.45	
For VIO=3.3V: SDIO Interface I/O Pins					
Input high voltage		VIH	0.625xVIO		
Input low voltage		VIL		0.25xVIO	
Output high voltage	@ 2 mA	VOH	0.75xVIO		
Output low voltage	@ 2 mA	VOL		0.125xVIO	
For VIO=1.8V; Other Digital I/O Pins					
Input high voltage		VIH	0.65xVIO		
Input low voltage		VIL		0.35xVIO	
Output high voltage	@ 2 mA	VOH	VIO-0.45		
Output low voltage	@ 2 mA	VOL		0.45	
For VIO=3.3V: Other Digital I/O Pins					
Input high voltage		VIH	2		
Input low voltage		VIL		0.8	
Output high voltage	@ 2 mA	VOH	VIO-0.4		
Output low voltage	@ 2 mA	VOL		0.4	

Table 15: Recommended Operating Conditions

9. Bluetooth RF Specifications

• VBAT = 3.6V
• Ambient temperature +25°C

9.1 Receive

Parameter	Condition	Min	Typ	Max	Unit
General					
BT BR, EDR operation frequency range		2402		2480	MHz
BT BR, EDR channel spacing			1		MHz
BT BR, EDR input impedance			50		Ω
BT BR, EDR sensitivity	BR, BER = 0.1%		-90		dBm
	EDR2, BER = 0.01%		-91		
	EDR3, BER = 0.01%		-86		
Input IP3		-15			dBm
Maximum input at antenna				-19	dBm
RX LO Leakage					
2.4G Band			-90		dBm
Interference Performance					
C/I co-channel	GFSK		8		dB
C/I 1-MHz adjacent channel	GFSK		-7		dB
C/I 2-MHz adjacent channel	GFSK		-38		dB
C/I ≥ 3-MHz adjacent channel	GFSK		-56		dB
C/I image channel	GFSK		-31		dB
C/I 1-MHz adjacent to image	GFSK		-56		dB
C/I co-channel	EDR2		9		dB
C/I 1-MHz adjacent channel	EDR2		-11		dB
C/I 2-MHz adjacent channel	EDR2		-39		dB
C/I ≥ 3-MHz adjacent channel	EDR2		-55		dB
C/I image channel	EDR2		-23		dB
C/I 1-MHz adjacent to image	EDR2		-43		dB
C/I co-channel	EDR3		17		dB
C/I 1-MHz adjacent channel	EDR3		-4		dB
C/I 2-MHz adjacent channel	EDR3		-37		dB
C/I ≥ 3-MHz adjacent channel	EDR3		-53		dB
C/I image channel	EDR3		-16		dB
C/I 1-MHz adjacent to image	EDR3		-37		dB

Table 16：sensitivity and Interference Performance

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-BandBlockingPerformance(CW)					
30–2000MHz	0.1%BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000MHz–12.75GHz	0.1%BER	–	–10.0	–	dBm
Out-of-BandBlockingPerformance,ModulatedInterferer					
		GFSK (1 Mbps)[b]			
698–716 MHz	WCDMA	–	–13.5	–	dBm
776–849 MHz	WCDMA	–	–13.8	–	dBm
824–849 MHz	GSM850	–	–13.5	–	dBm
824–849 MHz	WCDMA	–	–14.3	–	dBm
880–915 MHz	E-GSM	–	–13.1	–	dBm
880–915 MHz	WCDMA	–	–13.1	–	dBm
1710–1785 MHz	GSM1800	–	–18.1	–	dBm
1710–1785 MHz	WCDMA	–	–17.4	–	dBm
1850–1910 MHz	GSM1900	–	–19.4	–	dBm
1850–1910 MHz	WCDMA	–	–18.8	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.7	–	dBm
1920–1980 MHz	WCDMA	–	–19.6	–	dBm
2010–2025 MHz	TD–SCDMA	–	–20.4	–	dBm
2500–2570 MHz	WCDMA	–	–20.4	–	dBm
2500–2570 MHz[e]	Band 7	–	–30.5	–	dBm

2300-2400 MHz [f]	Band 40	–	–34.0	–	dBm
2570–2620 MHz [c]	Band 38	–	–30.8	–	dBm
2545–2575 MHz [d]	XGP Band	–	–29.5	–	dBm
		π/4 *DPSK (2 Mbps)*[b]			
698–716 MHz	WCDMA	–	–9.8	–	dBm
776–794 MHz	WCDMA	–	–9.7	–	dBm
824–849 MHz	GSM850	–	–10.7	–	dBm
824–849 MHz	WCDMA	–	–11.4	–	dBm
880–915 MHz	E-GSM	–	–10.4	–	dBm
880–915 MHz	WCDMA	–	–10.2	–	dBm
1710–1785 MHz	GSM1800	–	–15.8	–	dBm
1710–1785 MHz	WCDMA	–	–15.4	–	dBm
1850–1910 MHz	GSM1900	–	–16.6	–	dBm
1850–1910 MHz	WCDMA	–	–16.4	–	dBm
1880–1920 MHz	TD-SCDMA	–	–17.9	–	dBm
1920–1980 MHz	WCDMA	–	–16.8	–	dBm
2010–2025 MHz	TD-SCDMA	–	–18.6	–	dBm
2500–2570 MHz	WCDMA	–	–20.4	–	dBm
2500–2570 MHz [e]	Band 7	–	–31.9	–	dBm
2300–2400 MHz [f]	Band 40	–	–35.3	–	dBm
2570-2620 MHz [c]	Band 38	–	–31.8	–	dBm
2545-2575 MHz [d]	XGP Band	–	–31.1	–	dBm
		8DPSK (3 Mbps)[b]			
698–716 MHz	WCDMA	–	–12.6	–	dBm
776–794 MHz	WCDMA	–	–12.6	–	dBm
824–849 MHz	GSM850	–	–12.7	–	dBm
824–849 MHz	WCDMA	–	–13.7	–	dBm
880–915 MHz	E-GSM	–	–12.8	–	dBm
880–915 MHz	WCDMA	–	–12.6	–	dBm
1710–1785 MHz	GSM1800	–	–18.1	–	dBm
1710–1785 MHz	WCDMA	–	–17.4	–	dBm
1850–1910 MHz	GSM1900	–	–19.1	–	dBm
1850–1910 MHz	WCDMA	–	–18.6	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.3	–	dBm
1920–1980 MHz	WCDMA	–	–18.9	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.4	–	dBm
2500–2570 MHz	WCDMA	–	–21.4	–	dBm
2500–2570 MHz [e]	Band 7	–	–31.0	–	dBm
2300–2400 MHz [f]	Band 40	–	–34.5	–	dBm
2570–2620 MHz [c]	Band 38	–	–31.2	–	dBm
2545–2575 MHz [d]	XGP Band	–	–30.0	–	dBm

Table 17：Out-of-Band Blocking Performance

c. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
d. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
e. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
f. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.

Parameter	Conditions	Minimum	Typical	Maximum	Unit
SpuriousEmissions					
30MHz–1 GHz		–	–95	–62	dBm
1–12.75GHz		–	–70	–47	dBm
851–894MHz		–	–147	–	dBm/Hz
925–960MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170MHz		–	–147	–	dBm/Hz

Table 18：spurious emission

9.2 Transmitter

Parameter	Min	Typ	Max	BT Spec	Unit
BR RF output power		10			dBm
EDR RF output power		6			dBm
BR Power Control Step	2	4	8	2 to 8	dB
–20 dBc BW		0.93		≤ 1	MHz
EDR Adjacent Channel Power |M-N| = 1		-38		≤ -26	dBm
EDR Adjacent Channel Power |M-N| = 2		-31		≤ -20	
EDR Adjacent Channel Power |M-N| ＞2		-43		≤ -40	

Table 19：BT Transmitter

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-BandSpuriousEmissions					
30MHz to1GHz	–	–	–	–36.0	dBm
1GHzto 12.75GHz	–	–	–	–30.0	dBm
1.8GHzto1.9GHz	–	–	–	–47.0	dBm
5.15GHzto 5.3GHz	–	–	–	–47.0	dBm
GPSBandSpuriousEmission					
Spurious emissions	–	–	–103	–	dBm

Table 20：Spurious Emissions

Transmitted power in cellular isn't defined.

Parameter	Minimum	Typical	Maximum	Unit
LOPerformance				
Lock time	–	72	–	μs
Initial carrier frequency tolerance	–	±25		kHz
FrequencyDrift				
DH1packet	–	±8		kHz
DH3packet	–	±8		kHz
DH5packet	–	±8		kHz
Driftrate	–	5		kHz/50μs
FrequencyDeviation				
00001111sequenceinpayload[a]		155		kHz
10101010sequencein payload[b]		140	–	kHz
Channel Spacing	–	1	–	kHz

Table 21：Modulation

Parameter	Condition	Min	Typ	Max	Unit
frequency range		2402		2480	MHz
RX Sense(Dirty Tx on)	GFSK, 0.1% BER, 1		-91		dBm
TX Power			7		dBm
Mod Char: delta F1 average			250		KHz
Mod Char: delta F2 max			100		%
Mod Char: ratio			0.95		%

Table 22：BLE RF

10. WLAN RF Specifications

10.1 Introduction

The device includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radio.

• VBAT = 3.6V
• Ambient temperature +25°C

10.2 2.4 GHz Band General RF Specifications

Item	Condition	Typical	Maximum	Unit
TX/RXswitchtime	IncludingTX rampdown–	–	5	µs
RX/TXswitchtime	IncludingTX rampup –	–	2	µs
Power-up andpower-downramp time	DSSS/CCKmodulations–	–	<2	µs

Table 23：2.4 GHz Band General RF Specifications

10.3 WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency range		2400		2480	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1Mbps DSSS		-96		dBm
	11Mbps CCK		-88		
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6Mbps OFDM		-92		
	54Mbps OFDM		-74		
RX sensitivity IEEE 802.11n 20M (10% PER for 4096 octet PSDU) default parameters: 800 ns GI and non-STBC	MCS0		-89		
	MCS7		-73		
RX sensitivity IEEE 802.11n 40M (8% PER for 4096 octet PSDU default parameters: 800 ns GI and non-STBC)	MCS0 40MHz		TBD		
	MCS7 40MHz		TBD		
RX sensitivity IEEE 802.11ac 20M (10% PER for 4096 octet PSDU) default parameters: 800 ns GI and non-STBC	MCS0		-89		
	MCS8		-69		

RX sensitivity IEEE 802.11ac 40M(10% PER for 4096 octet PSDU) default parameters: 800 ns GI and non-STBC	MCS0		TBD		
	MCS9		TBD		
RX sensitivity IEEE 802.11ac 80M(10% PER for 4096 octet PSDU) 800 ns GI, LDPC coding, and non- STBC.	MCS9		TBD		
Max Input Level	11b (8% PER, 1024 octets)	-9.5			dBm
	11g(10% PER, 1024 octets)	-9.5			
	M0-M7(10% PER, 4096 octets)	-9.5			
	M8-M9(10% PER, 4096 octets)	-11.5			

Table 24：2.4GHz Sensitivity and Max Input Level

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blockinglevelfor3dBRX sensitivitydegradation (without external filtering)	776–794MHz	CDMA200	–	–24	–	dBm
	824–849MHz[g]	cdmaOne	–	–25	–	dBm
	824–849MHz	GSM850	–	–15	–	dBm
	880–915MHz	E-GSM	–	–16	–	dBm
	1710–1785MHz	GSM1800	–	–18	–	dBm
	1850–1910MHz	GSM1800	–	–19	–	dBm
	1850–1910MHz	cdmaOne	–	–26	–	dBm
	1850–1910MHz	WCDMA	–	–26	–	dBm
	1920–1980MHz	WCDMA	–	–28.5	–	dBm
	2500–2570MHz	Band 7	–	–45	–	dBm
	2300–2400MHz	Band 40	–	–50	–	dBm
	2570–2620MHz	Band 38	–	–45	–	dBm
	2545–2575MHz	XGPBand	–	–45	–	dBm

Adjacent channel rejection—DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection—OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
	MCS8	–59 dBm	–4	–	–	dB
	MCS9	–57 dBm	–6	–	–	dB

Table 25：Block And Adjacent channel rejection

10.4 WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition	EVM	Min	Typ	Max	Unit
TX powerat 25°C and VBAT=3.6V withspectral maskand EVM compliance[a,b]	802.11b (DSSS/CCK)	-9		17		dBm
	OFDM, BPSK	-8		16		dBm
	OFDM, QPSK	-13		16		dBm
	OFDM, 16-QAM	-19		15		dBm
	OFDM, 64-QAM (R = 3/4)	-25		15		dBm
	OFDM, 64-QAM (MCS7, HT20)	-28		15		dBm
	OFDM, 256-QAM (MCS8, VHT20)	-30		13		dBm
	OFDM, 256-QAM (MCS8, VHT40)	-32		TBD		dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz			0.45		Degrees RMS

Table 26：2.4GHz Power And EVM

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequencyrange	–		2400	–	2500	MHz
Transmittedpower in cellular andFM bands (at16.5dBm,100% duty cycle,1Mbps CCK)[a]	76–108MHz	FM RX	–	–148.5	–	dBm/Hz
	776–794MHz	–	–	–126.5	–	dBm/Hz
	869–960MHz	cdmaOne,GSM850	–	–162.5	–	dBm/Hz
	925–960MHz	E-GSM	–	–162.5	–	dBm/Hz
	1570–1580MHz	GPS	–	–149.5	–	dBm/Hz
	1805–1880MHz	GSM1800	–	–140.5	–	dBm/Hz
	1930–1990MHz	GSM1900,cdmaOne,WCDMA	–	–137.5	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–128.5	–	dBm/Hz
	2500–2570MHz	Band7	–	–104.5	–	dBm/Hz
	2300–2400MHz	Band40	–	–94.5	–	dBm/Hz
	2570–2620MHz	Band38	–	–119.5	–	dBm/Hz
	2545–2575MHz	XGPBand	–	–109.5	–	dBm/Hz

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
TXpowercontroldynamic range	–	10	–	–	dB
Closed-loopTXpower variationat highest power levelsetting	Across fulltemperatureand voltagerange	–	±1.5	–	dB
Carrier suppression	–	15	–	–	dBc
Gaincontrolstep	–	–	0.25	–	dB
Returnlossat ChipportTX	Z_o= 50Ω	–	6	–	dB

Table 27：2.4GHz TX Performance

a. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.
b. TX power for Channel 1 and Channel 11 is specified by nonvolatile memory parameters.

10.5 5 GHz Receiver Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency range		4900		5845	MHz
RX sensitivity IEEE 802.11a (10% PER for 1024 octet PSDU)[a]	6Mbps OFDM		-92		dBm
	54Mbps OFDM		-74		
RX sensitivity IEEE 802.11n 20M (10% PER for 4096 octet PSDU)[a] default parameters: 800 ns GI and non-STBC	MCS0		-90		
	MCS7		-73		
RX sensitivity IEEE 802.11n 40M (8% PER for 4096 octet PSDU)[a]default parameters: 800 ns GI and non-STBC	MCS0 40MHz		-88		
	MCS7 40MHz		-69		
RX sensitivity IEEE 802.11ac 20M (10% PER for 4096 octet PSDU)[a] default parameters: 800 ns GI and non-STBC	MCS0		-89		
	MCS8		-68		
RX sensitivity IEEE 802.11ac 40M(10% PER for 4096 octet PSDU)[a] default parameters: 800 ns GI and non-STBC	MCS0		-88		
	MCS9		-63		
RX sensitivity IEEE 802.11ac 80M(10% PER for 4096 octet PSDU) [a]800 ns GIand non- STBC.	MCS0		-85		
	MCS9		-58		
Max Input Level	11g	-15			dBm
	11n/ac	-20			

Table 28：5GHz Sensitivity and Max Input Level

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 1 dBRX sensitivity degradation[b]	824-849 MHz	cdmaOne	-20	-	-	dBm
	824-849 MHz	GSM850	–12	-	-	
	880–915MHz	E-GSM	–12	–	–	dBm
	1710–1785MHz	GSM1800	–15	–	–	dBm
	1850–1910MHz	GSM1800	–15	–	–	dBm
	1850–1910MHz	cdmaOne	–20	–	–	dBm
	1850–1910MHz	WCDMA	–21	–	–	dBm
	1920–1980MHz	WCDMA	–21	–	–	dBm
	2500–2570MHz	Band 7	–21	–	–	dBm
	2300–2400MHz	Band 40	–21	–	–	dBm

	2570–2620MHz	Band 38	–21	–	–	dBm
	2545–2575MHz	XGPBand		–21		–
Inputin-bandIP3[a]	MaximumLNAgain		–	TBD	–	–
	MinimumLNAgain		–	TBD	–	–
Maximumreceivelevel@5.24GHz	@6, 9,12Mbps		–9.5	–	–	dBm
	@18,24,36,48,54 Mbps		–14.5	–	–	dBm
LPF3dBbandwidth	–			TBD		MHz
Adjacentchannelrejection(Difference between interferinganddesired signal (20MHzapart)at 10% PERfor1000 octet PSDUwithdesiredsignal levelasspecifiedin Condition/Notes)	6MbpsOFDM	–79dBm	16	–	–	dBm
	9MbpsOFDM	–78dBm	15	–	–	dBm
	12Mbps OFDM	–76dBm	13	–	–	dBm
	18Mbps OFDM	–74dBm	11	–	–	dBm
	24Mbps OFDM	–71dBm	8	–	–	dBm
	36Mbps OFDM	–67dBm	4	–	–	dBm
	48Mbps OFDM	–63dBm	0	–	–	dBm
	54Mbps OFDM	–62dBm	–1	–	–	dBm
	65Mbps OFDM	–61dBm	–2	–	–	dBm

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Alternateadjacentchannel rejection (Difference between intefering and desired signal(40MHzapart)at 10% PERfor1000[c]octet PSDUwithdesiredsignal Condition/Notes)	6MbpsOFDM	–	32	–	–	dB
	9MbpsOFDM	–77.5dBm	31	–	–	dB
	12Mbps OFDM	–75.5dBm	29	–	–	dB
	18Mbps OFDM	–73.5dBm	27	–	–	dB
	24Mbps OFDM	–70.5dBm	24	–	–	dB
	36Mbps OFDM	–66.5dBm	20	–	–	dB
	48Mbps OFDM	–62.5dBm	16	–	–	dB
	54Mbps OFDM	–61.5dBm	15	–	–	dB
	65Mbps OFDM	–60.5dBm	14	–	–	dB

Table 29：Block And Alternate adjacent channel rejection

a. Derate by 1.5 dB for –40°C to –10°C and 55°C to 85°C.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. For 65 Mbps, the size is 4096.

10.6 WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition	EVM	Min	Typ	Max	Unit
TX powerat 25°C and VBAT=3.6V withspectral maskand EVM compliance[a,b]	OFDM, QPSK	-13		17		dBm
	OFDM, 16-QAM	-19		15		dBm
	OFDM, 64-QAM (R = 3/4)	-25		15		dBm
	OFDM, 64-QAM (MCS7, HT20)	-27		15		dBm
	OFDM, 256-QAM (MCS8, VHT20)	-30		13		dBm
	OFDM, 256-QAM (MCS9, VHT40)	-32		13		dBm
	OFDM, 256-QAM (MCS9, VHT80)	-32		12		
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz			0.45		Degrees RMS
TXpowercontrol dynamic range	——		10			dB

Table 30：5GHz Power And EVM

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequencyrange	–		4900	–	5845	MHz
Transmittedpower in cellular andFM bands(at18.5dBm)[a]	76–108MHz	FMRX	–	–161.5	–	dBm/Hz
	776–794MHz	–	–	–161.5	–	dBm/Hz
	869–960MHz	cdmaOne, GSM850	–	–161.5	–	dBm/Hz
	925–960MHz	E-GSM	–	–161.5	–	dBm/Hz
	1570–1580MHz	GPS	–	–161.5	–	dBm/Hz
	1805–1880MHz	GSM1800	–	–159.5	–	dBm/Hz
	1930–1990MHz	GSM1900 ,cdmaOne, WCDMA	–	–161.5	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–158.5	–	dBm/Hz
	2400–2483MHz	BT/WLAN	–	–156.5	–	dBm/Hz
	2500–2570MHz	Band7	–	–156.5	–	dBm/Hz
	2300–2400MHz	Band40	–	–156.5	–	dBm/Hz
	2570–2620MHz	Band38	–	–156.5	–	dBm/Hz
	2545–2575MHz	XGPband	–	–156.5	–	dBm/Hz
Parameter	**Condition/Notes**		**Minimum**	**Typical**	**Maximum**	**Unit**
ClosedloopTX power variationat highestpower levelsetting	Across full-temperatureandvoltage range.		–	±2.0	–	dB
Carrier suppression	–		15	–	–	dBc
Gaincontrolstep	–		–	0.25	–	dB
Returnloss	Z_0= 50Ω		–	6	–	dB

Table 31：5GHz TX Performance

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.
b. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.

10.7 General Spurious Emissions Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequencyrange	–		2400	–	2500	MHz
GeneralSpuriousEmissions						
TXemissions	30MHz <f<1GHz	RBW=100kHz	–	–93	–	dBm
	1GHz<f< 12.75GHz	RBW=1MHz	–	–45.5	–	dBm
	1.8 GHz<f < 1.9GHz	RBW= 1MHz	–	–72	–	dBm
	5.15GHz< f<5.3 GHz	RBW= 1MHz	–	–87	–	dBm
RX/standbyemissions	30MHz <f<1GHz	RBW=100kHz	–	–107	–	dBm
	1GHz<f< 12.75GHz	RBW=1MHz	–	–65[a]	–	dBm
	1.8 GHz<f < 1.9GHz	RBW= 1MHz	–	–87	–	dBm
	5.15GHz< f<5.3 GHz	RBW= 1MHz	–	–100	–	dBm

Table 32：General Spurious Emissions Specifications

a.The value presented in this table is the result of LO leakage at 3/2 * fc for 2.4 GHz or 2/3 * fc for 5 GHz (where fc is the carrier frequency). For all other emissions in this range, the value is –96 dBm.

11. System Power Consumption

11.1 WLAN Current Consumption

VBAT = 3.6V, VDDIO = 1.8V, TA 25°C

Mode	Bandwidth (MHz)	Band (GHz)	Typic mA VBAT	Max mA VBAT	TypicμA Vio[a]	Max μA Vio[a]
SleepModes						
OFF[b]	–	–	0.01	TBD	5	TBD
SLEEP[c]	–	–	0.015	TBD	150	TBD
IEEEPowerSave,DTIM1[d]	–	2.4	TBD	TBD	TBD	TBD
IEEEPowerSave,DTIM3[d]	–	2.4	TBD	TBD	TBD	TBD
IEEEPowerSave,DTIM1[d]	–	5	TBD	TBD	TBD	TBD
IEEEPowerSave,DTIM3[d]	–	5	TBD	TBD	TBD	TBD
ActiveModes						
Receive[e,f]MCS8(SGI)	20	2.4	TBD	TBD	TBD	TBD
Receive[e,f]MCS7(SGI)	20	5	TBD	TBD	TBD	TBD
Receive[e,f]MCS7(SGI)	40	5	TBD	TBD	TBD	TBD
Receive[e,f]MCS9(SGI)	80	5	TBD	TBD	TBD	TBD

Table 33：WLAN Current Consumption

a. VIOisspecifiedwithallpinsidle(notswitching)andnotdrivinganyloads.

b. WL_REG_ON,BT_REG_ONlow.

c. Idle,notassociated,or inter-beacon.

d. Beacon Interval= 102.4 ms.Beaconduration= 1 ms @1Mbps.Average current over the specifiedDTIM intervals.

e. Measuredusingpacketenginetestmode.

f. Dutycycleis100%.Carrier sense(CS)detect/packetreceive.

11.2 BT Current Consumption

Operating Mode	Typical VBAT (VBAT=3.3V)	MaxVBAT (VBAT=3.3V)	Typical VIO (VIO=1.8V)	MaxVIO (VIO=1.8V)	Units
Sleep	15	TBD	225	TBD	μA

Table 34：WLAN Current Consumption

12. Interface Timing

12.1 SDIO Timing

12.1.1 SDIO Default Mode Timing

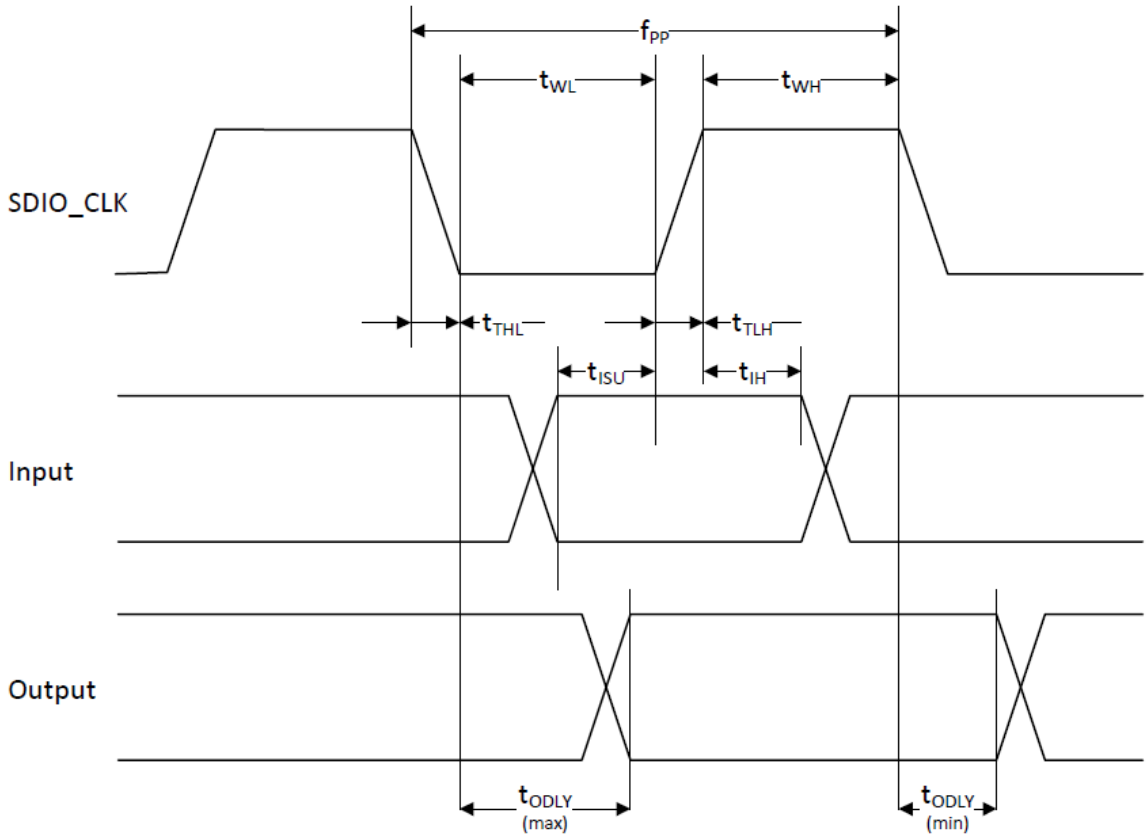


Figure 24：SDIO Default Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIOCLK(AllvaluesarereferredtominimumVIHandmaximumVIL[b])					
Frequency– DataTransfermode	fPP	0	–	25	MHz
Frequency– Identificationmode	fOD	0	–	400	kHz
Clocklowtime	tWL	10	–	–	ns
Clockhightime	tWH	10	–	–	ns
Clockrisetime	tTLH	–	–	10	ns
Clockfall time	tTHL	–	–	10	ns

Inputs:CMD,DAT(referencedtoCLK)					

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Inputsetuptime	tISU	5	–	–	ns
Inputholdtime	tIH	5	–	–	ns
Outputs:CMD,DAT(referencedtoCLK)					
Outputdelay time–DataTransfermode	tODLY	0	–	14	ns
Outputdelay time–Identificationmode	tODLY	0	–	50	ns

Table 35：SDIOBusTiming[a]Parameters(DefaultMode)(Cont.)

a. TimingisbasedonCL≤40pFloadonCMDandData.

b. Min.(Vih) =0.7× VIOand max(Vil)= 0.2 ×VIO.

12.1.2 SDIO High-Speed Mode Timing

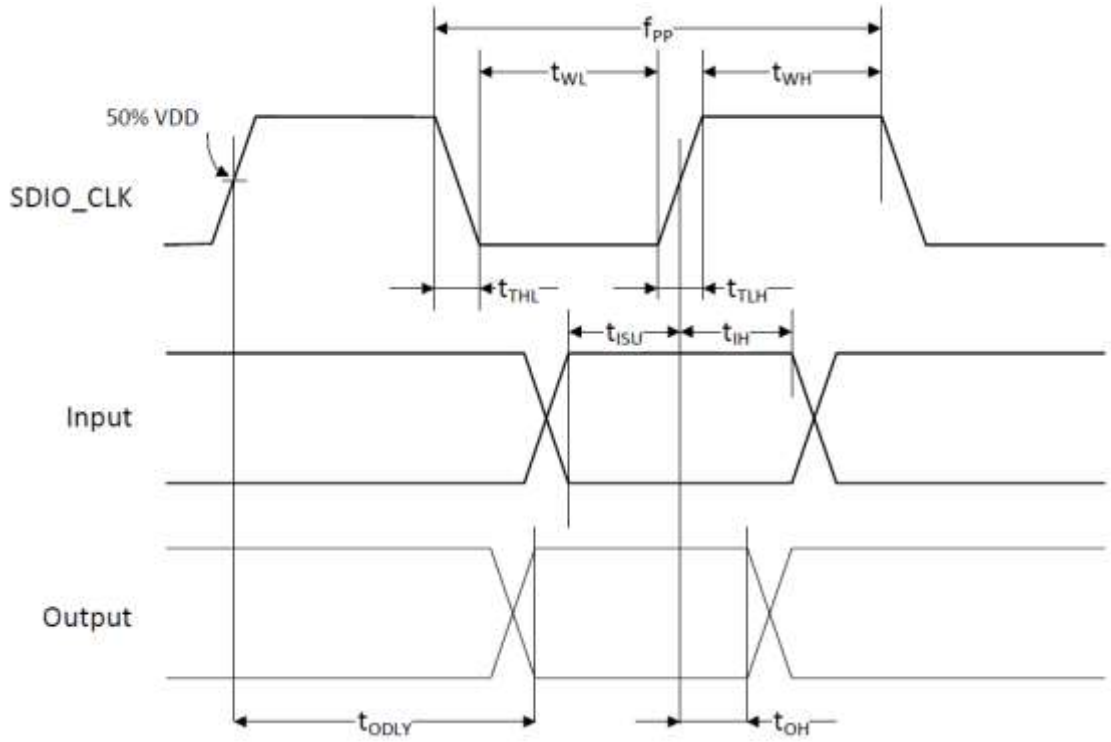


Figure 25: SDIO Bus Timing (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximu	Unit
SDIOCLK(allvaluesarereferredtominimumVIHandmaximumVI L[b])					
Frequency– DataTransferMode	fPP	0	–	50	MHz
Frequency– IdentificationMode	fOD	0	–	400	kHz

Clocklowtime	tWL	7	–	–	ns
Clockhightime	tWH	7	–	–	ns
Clockrisetime	tTLH	–	–	3	ns
Clockfall time	tTHL	–	–	3	ns
Inputs:CMD,DAT(referencedtoCLK)					
Inputsetuptime	tISU	6	–	–	ns
Inputholdtime	tIH	2	–	–	ns
Outputs:CMD,DAT(referencedtoCLK)					
Outputdelay time–DataTransferMode	tODLY	–	–	14	ns
Outputholdtime	tOH	2.5	–	–	ns
Totalsystemcapacitance(eachline)	CL	–	–	40	pF

Table 36:SDIO Bus Timing[a] Parameters (High-Speed Mode)

a. TimingisbasedonCL≤40pFloadonCMDandData.

b. Min.(Vih) =0.7× VIOand max(Vil)= 0.2 ×VIO.

12.1.3 SDIO Bus Timing Specifications in SDR Modes

12.1.3.1 Clock Timing

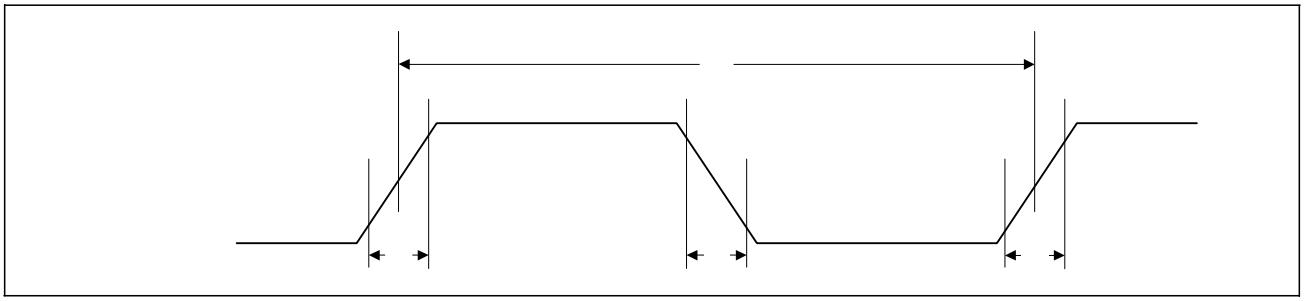


Figure 26:SDIO Clock Timing (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR},t_{CF}	–	0.2 ×t_{CLK}	ns	t_{CR},t_{CF}<2.00ns (max.)@100MHz, C_{CARD}= 10pF t_{CR},t_{CF}<0.96ns (max.)@208MHz, C_{CARD}= 10pF
Clockduty cycle	–	30	70	%	–

Table 37: SDIOBusClockTimingParameters(SDRModes)

12.1.3.2 Device Input Timing Timing

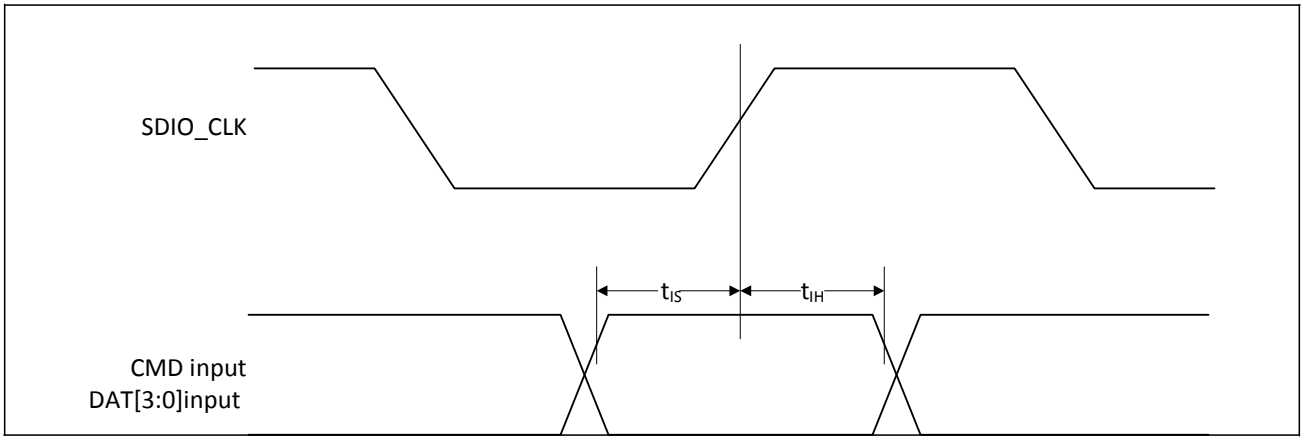


Figure 27:SDIO Bus Input Timing (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104Mode				
t_{IS}	1.4	–	ns	C_{CARD}= 10pF, VCT= 0.975V
t_{IH}	0.8	–	ns	C_{CARD}= 5 pF,VCT=0.975V
SDR50Mode				
t_{IS}	3.0	–	ns	C_{CARD}= 10pF, VCT= 0.975V
t_{IH}	0.8	–	ns	C_{CARD}= 5 pF,VCT=0.975V
SDR25Mode				
t_{IS}	3.0	–	ns	C_{CARD}= 10pF, VCT= 0.975V
t_{IH}	0.8	–	ns	C_{CARD}= 5 pF,VCT=0.975V
SDR12Mode				
t_{IS}	3.0	–	ns	C_{CARD}= 10pF, VCT= 0.975V
t_{IH}	0.8	–	ns	C_{CARD}= 5 pF,VCT=0.975V

Table 38: SDIO Bus Input Timing Parameters (SDR Modes)

12.1.3.3 Device Output Timing

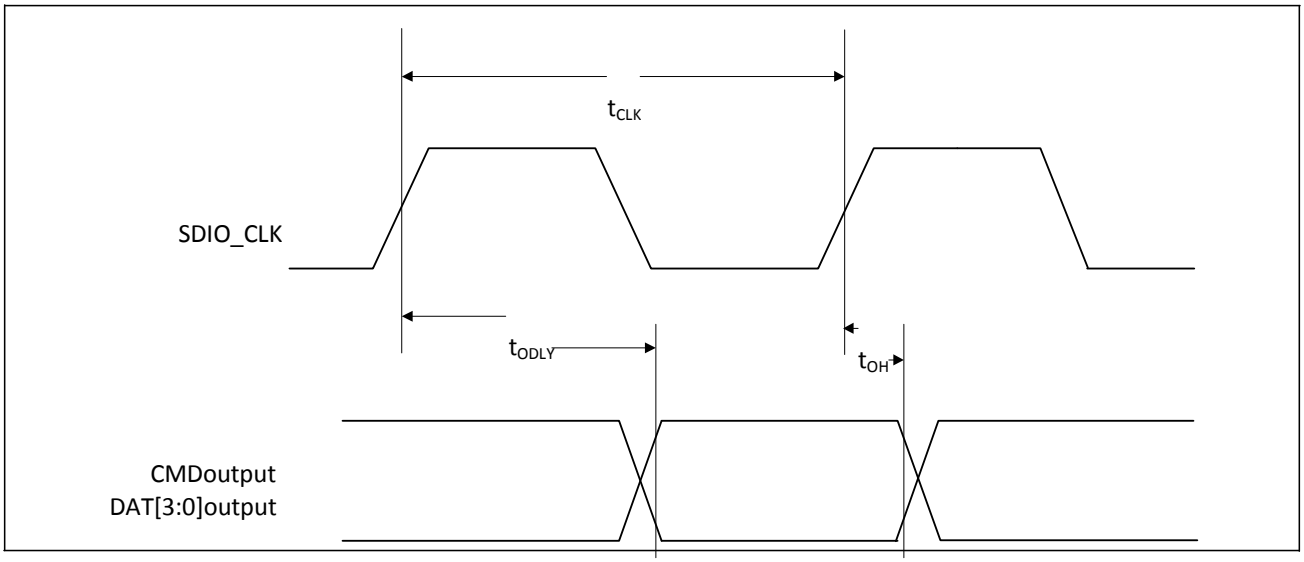


Figure 28: SDIOBusOutputTiming(SDRModesupto100MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK}≥10nsC_L=30pFusingdrivertypeBforSDR50
t_{ODLY}	–	14.0	ns	t_{CLK}≥ 20ns C_L= 40pFusing forSDR12,SDR25
t_{OH}	1.5	–	ns	Holdtime at thet_{ODLY}(min) C_L= 15 pF

Table 39：SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

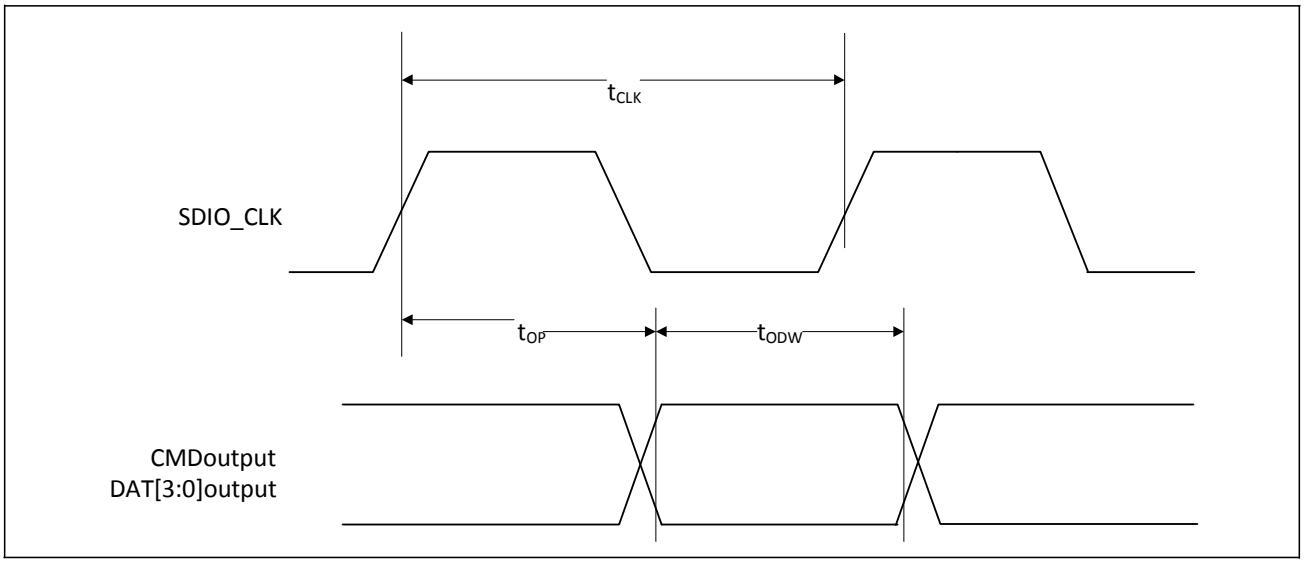


Figure 29：SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Cardoutputphase
Δt_{OP}	–350	+1550	ps	Delay variationdue to tempchangeaftertuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88ns @208MHz

Table 40：SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

- Δt_{OP}= +1550psforjunctiontemperature ofΔt_{OP}=90 degrees duringoperation
- Δt_{OP}= –350psforjunction temperatureof Δt_{OP}= –20degrees duringoperation
- Δt_{OP}= +2600psforjunctiontemperature ofΔt_{OP}=–20to+125 degrees duringoperation

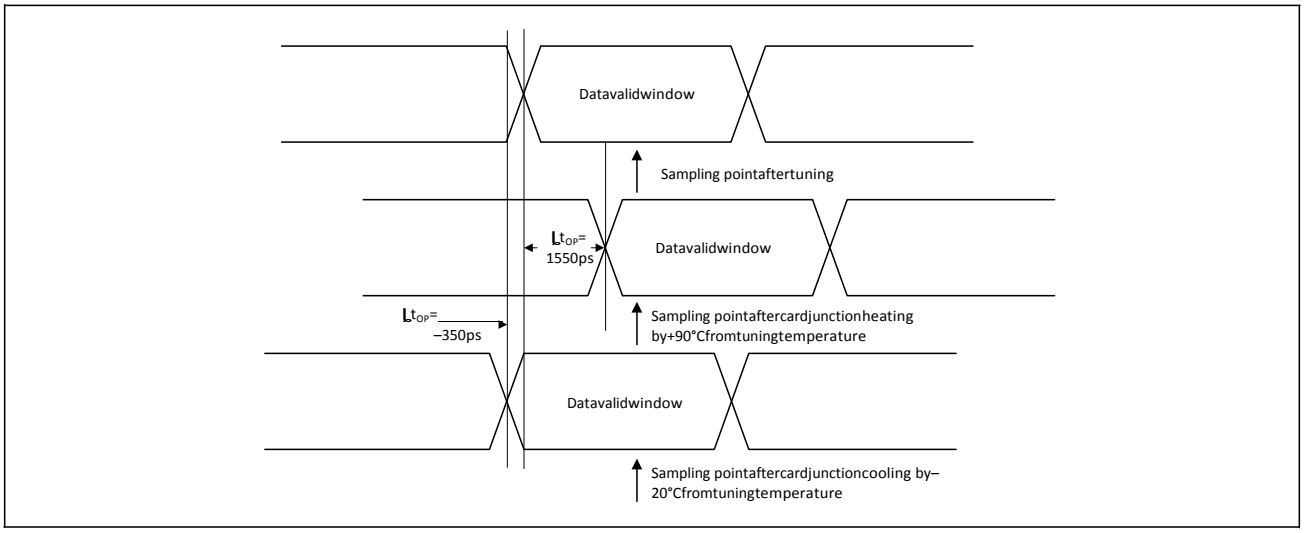
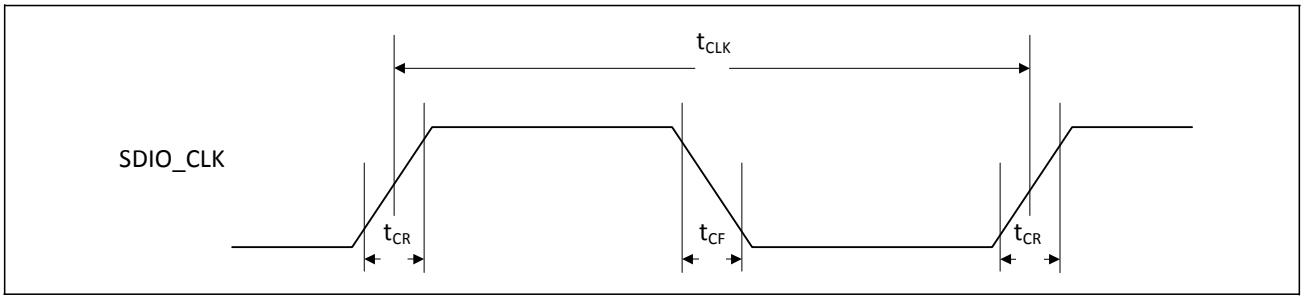


Figure 30：ΔtOP Consideration for Variable Data Window (SDR 104 Mode)

12.1.4 SDIO Bus Timing Specifications in DDR50 Mode

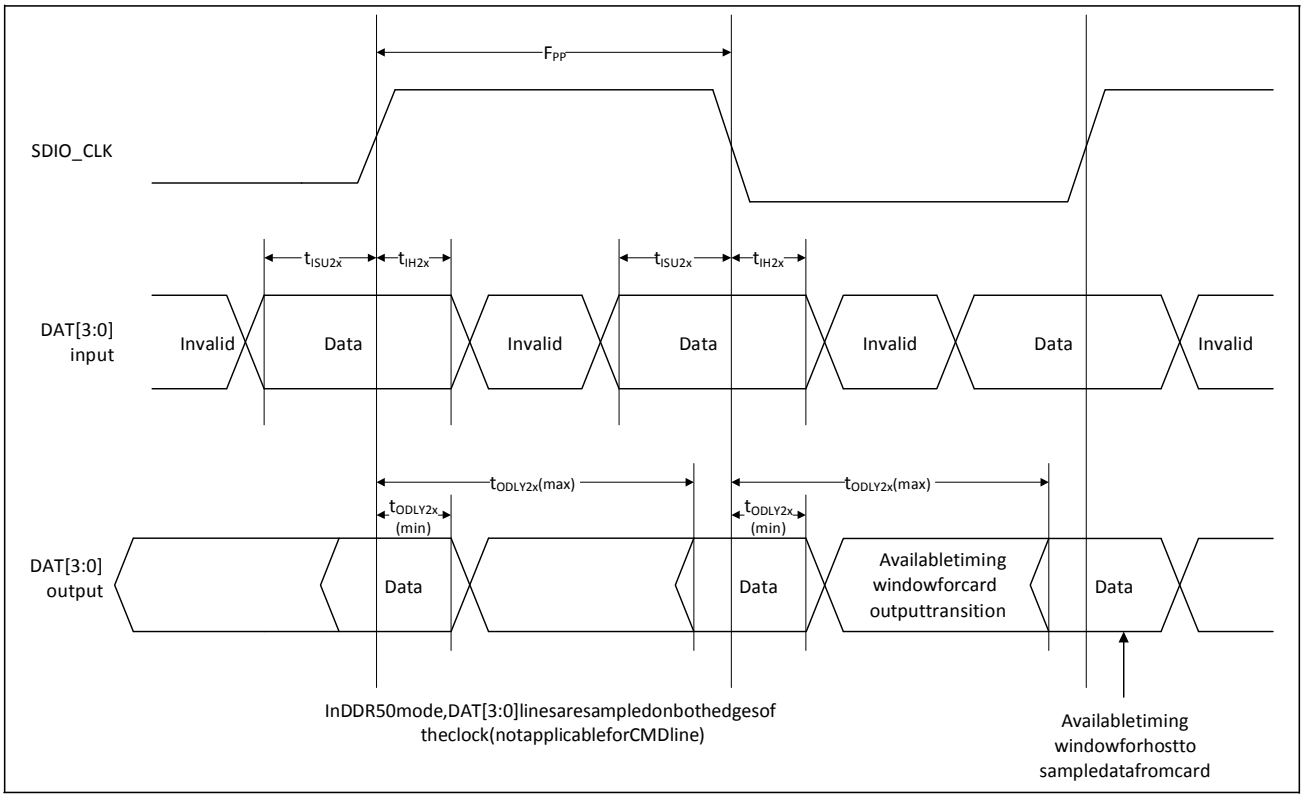


Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50mode

–	t_{CR},t_{CF}	–	0.2×tCLK	ns	t_{CR},t_{CF}< 4.00ns(max) @50MHz, C_{CARD}=10 pF
Clockduty cycle	–	45	55	%	–

Table 41：SDIO Bus Clock Timing Parameters (DDR50 Mode)

12.1.5 Data Timing, DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
InputCMD					
Inputsetuptime	t_{ISU}	6	–	ns	C_{CARD}<10pF(1Card)
Inputholdtime	t_{IH}	0.8	–	ns	C_{CARD}<10pF(1Card)
OutputCMD					
Outputdelay time	t_{ODLY}	–	13.7	ns	C_{CARD}<30pF(1Card)
Outputholdtime	t_{OH}	1.5	–	ns	C_{CARD}<15pF(1Card)
InputDAT					
Inputsetuptime	t_{ISU2x}	3	–	ns	C_{CARD}<10pF(1Card)
Inputholdtime	t_{IH2x}	0.8	–	ns	C_{CARD}<10pF(1Card)
OutputDAT					
Outputdelay time	t_{ODLY2x}	–	7.0	ns	C_{CARD}<25pF(1Card)
Outputholdtime	t_{ODLY2x}	1.5	–	ns	C_{CARD}<15pF(1Card)

Table 42：SDIO Bus Timing Parameters (DDR50 Mode)

13. Reference Design

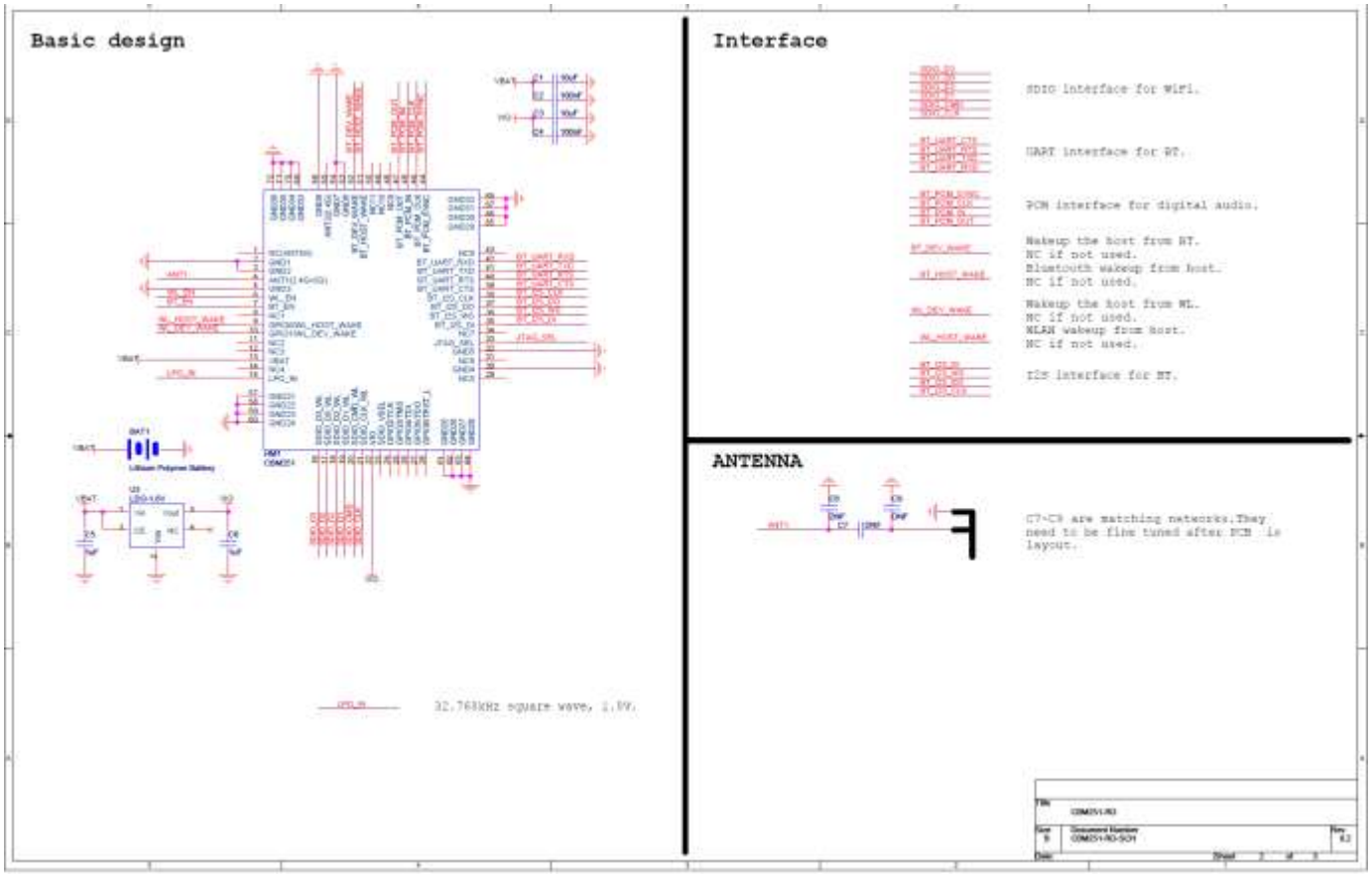


Figure 31:CBM251IQ2A/AQ2A Reference Design

14. Mechanical Characteristic

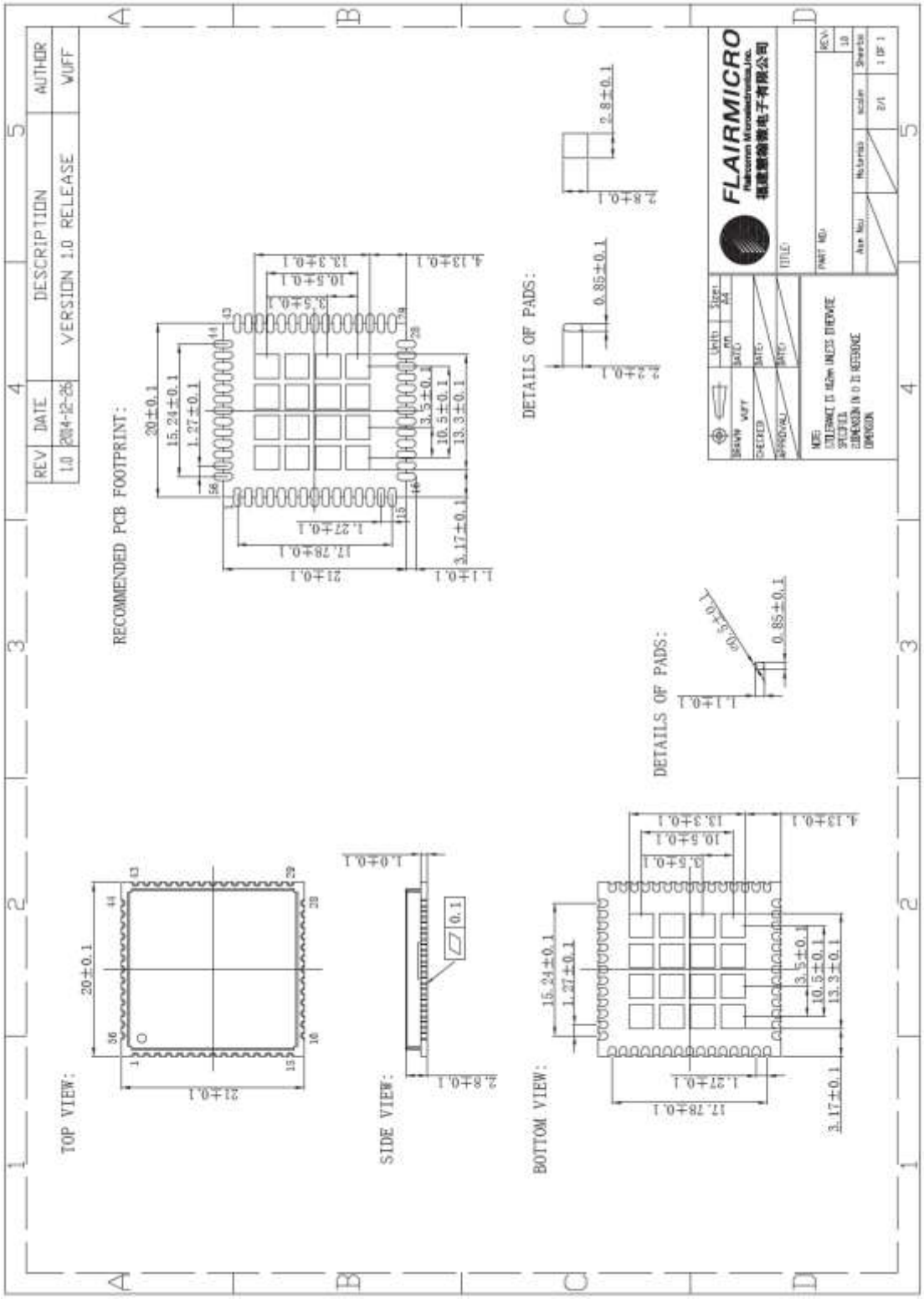


Figure 32：CBM251IQ2A/AQ2A Mechanical Characteristic

15. Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in Figure 33 below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

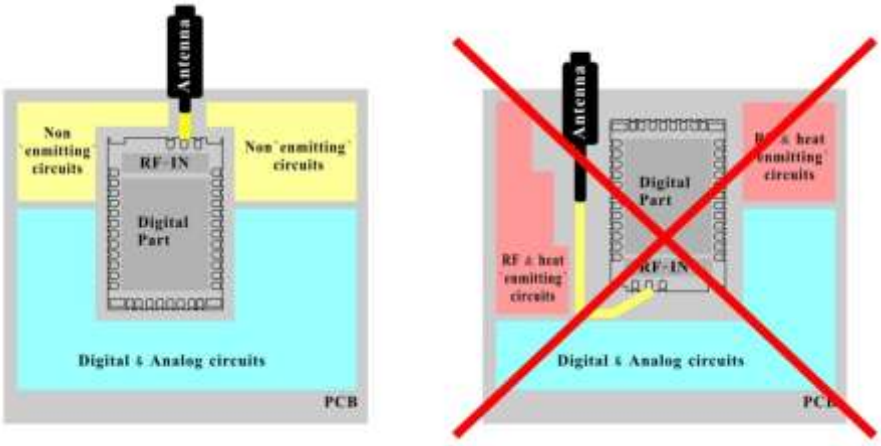


Figure 33:Placement the Module on a System Board

15.1 Antenna Connection and Grounding Plane Design

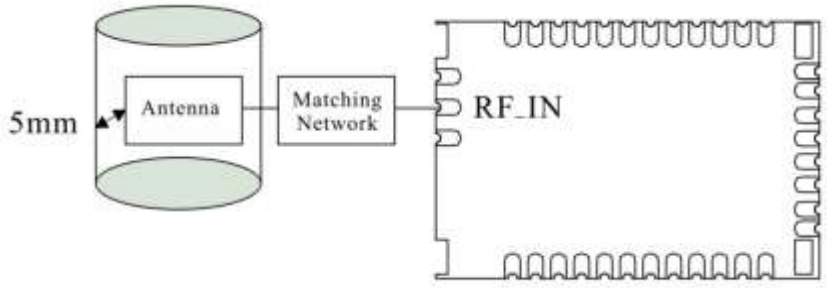


Figure 34: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and groundarea on thetop layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

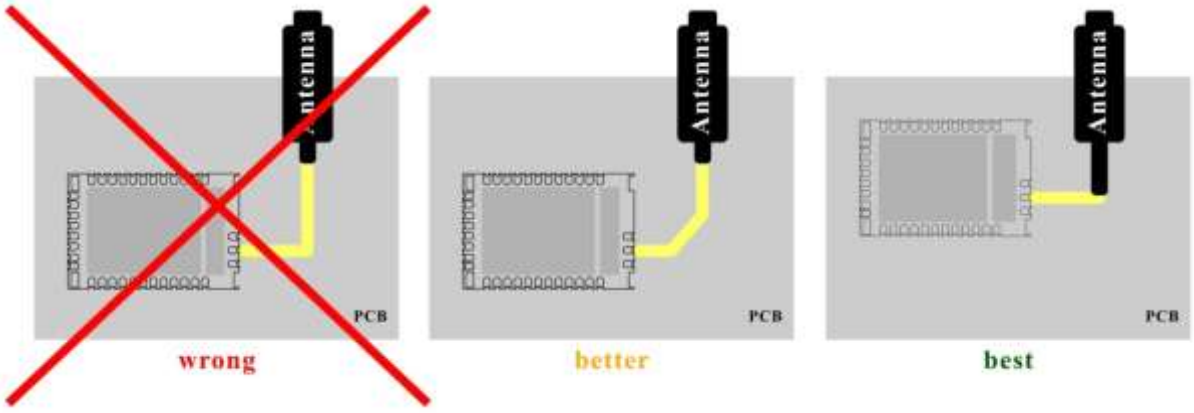


Figure 35: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

16. Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

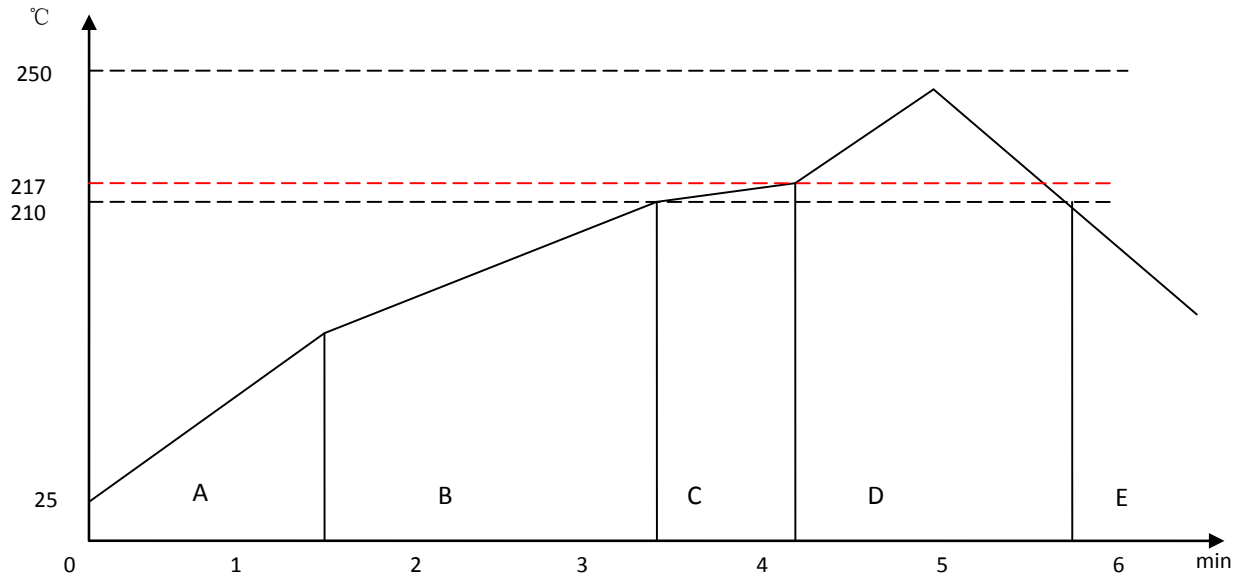


Figure 36: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone**.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C**.

17. Ordering Information

17.1 Product Packaging Information

TBD

Figure 37: Product Packaging Information

17.2 Ordering information

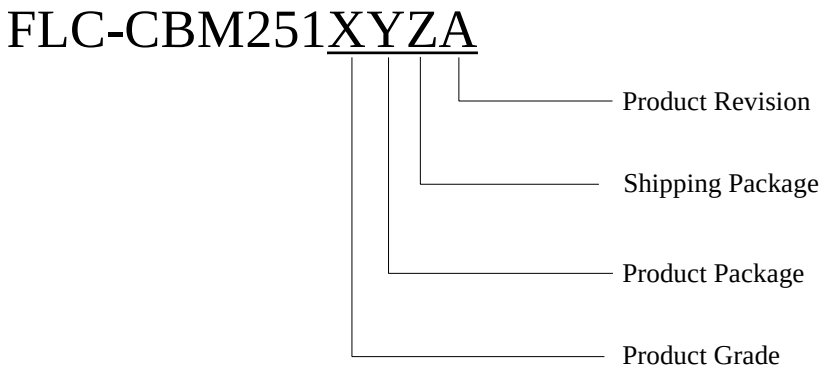


Figure 38: Ordering Information

Package		Order Number
Type	Shipment	CBM251IQ2A / AQ2A
QFN	Tape and reel	

Table 43: Ordering Information

17.2.1 Product Revision

Product Revision	Description	Availability
A	WL/BT Shared Antenna	Yes
B	2.4G and 5G Dual Antenna	TBD

Table 44: Product Revision

17.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	—	No

1	Plastic Tray	—	No
2	Reel	600	Yes

Table 45: Shipping Package

17.2.3 Product Package

Product Package	Description	Availability
Q	QFN	Yes
L	LGA	No
B	BGA	No
C	Connector	No

Table 46: Product Package

17.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	No
I	Industrial	No
V	Automobile After-Market	No
A	Automobile Before-Market	Yes

Table 47: Product Grade