CMOS LIS of Real Time Watch with Serial Interface

IN1363

FEATURES

- Count of seconds, minutes, hours, week days, date, months and years with consideration of leap years (until 2100);
- 400 kHz, double wire serial interface;
- Programmed orthogonal output signal;
- Function programming of alarm, timer and interruption;
- Automatic determination of the supply voltage drop;
- Consumption current of less, than 450 nA with supply of 2V with the operating oscillator;
- Operating temperature range: -40°C – +85°C.

SOP- 8

MSOP-8

TA = - 40 ... + 85 °C
for all packages

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
IN1363DT	T_A = - 40 ... + 85 °C	SOP-8	Tape & Reel
IN1363D		SOP-8	Tube
IN1363MDT		MSOP-8	Tape & Reel
IN1363MD		MSOP-8	Tube

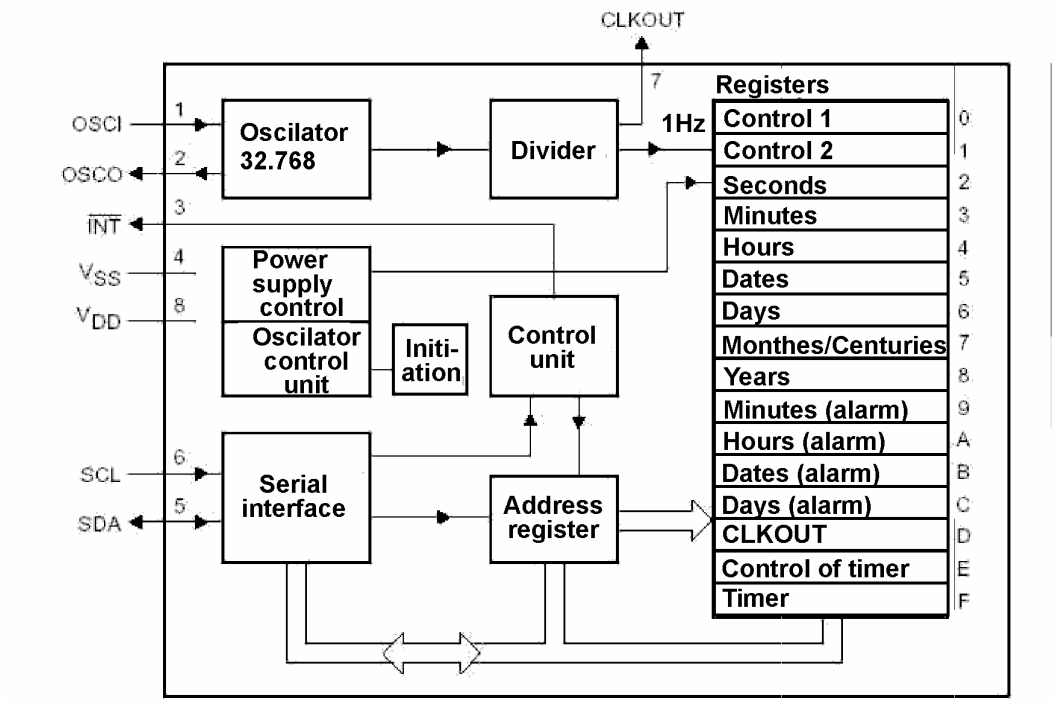
DESCRIPTION

Microcircuit IN1363 is essentially the complete binary-decimal digital watch with calendar, alarm, timer and possesses low power consumption. Addresses and data are transferred in series via the double wire bi-directional bus. The microcircuit is intended for count of real time in hours, minutes and seconds, count of week days, date, month and year. The last day of the month is automatically adjusted for the months with fewer, than 31 days, including correction for the leap year. The watch functions in the 24 hour mode. The microcircuit IN1363 has the built-in power control circuit, which determines the power level < 1V and forms the bit, signaling, that information about the real time may not be correct.

PINS DESCRIPTION

Pin Number	Symbol	Description
01	OSCI	Pin for connection of the quartz resonator
02	OSCO	Pin for connection of the quartz resonator
03	INT	Interruption output
04	V_{SS}	Common pin
05	SDA	Input / Output of data
06	SCL	Synchrosignal input
07	CLKOUT	Frequency divider output
08	V_{DD}	Supply source pin

BLOCK DIAGRAM



ASOLUTE MAXIMUM RATING

Limit and limit permissible operating modes of the microcircuit IN1363 are listed in the table

Characteristics	Symbol	Limit Permissible		Limit		Unit
		Min	Max	Min	Max	
Supply voltage	V_{DD}	1.0	5.5	–0.5	6.5	V
Dissipated power	P_{tot}	-	-	-	300	mWt
Input voltage SCL, SDA, OSCI	V_I	0	5.5	–0.5	6.5	V
Output voltage CLKOUT,INT	V_O	0	5.5	–0.5	6.5	V
Direct input or output current via any pin	I_{IO}	-	-	–10	10	mA

All voltages are listed relative to ground. Under influence of the limit mode serviceability of the microcircuits is not guaranteed. After plotting the limit mode serviceability is guaranteed in the limit permissible mode.

* Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.
These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = –40...+ 85°C, V_{CC} = 4,5 – 5,5 V)

Characteristics	Symbol	Test Condition	Min	Max	Note	Unit
Supply voltage	V_{DD}	I2C bus –active; F_{SCL} = 400 kHz	1.8	5.5		V
		in the non-active mode	1.0	5.5	1,2	
Input leakage current	I_{LI}	V_{IN} =V_{DD}; V_{IN} =V_{SS}	-	1		uA
Output leakage current	I_{LO}	V_{OUT} =V_{DD}; V_{OUT} =V_{SS}	-	1		uA
Consumption current	I_{DD1}	CLKOUT–off, F_{SCL} =400 kHz	-	800		uA
		CLKOUT–off, F_{SCL} =100 kHz	-	200		
		CLKOUT–off, F_{SCL} =0 kHz, V_{DD}=5V	-	0.55	1,2	
		CLKOUT–off, F_{SCL} =0 kHz, V_{DD}=2V	-	0.45	1,2	
Low level input voltage	V_{IL}		V_{SS}	$0.3V_{DD}$		V
High level input voltage	V_{IH}		$0.7V_{DD}$	V_{DD}		V
Low level output current at pin CLKOUT	I_{OL1}	V_{OL} = 0.4 V, V_{DD} =5 V	1	-		mA
High level output current at pin CLKOUT	I_{OH1}	V_{OH} = 4.6 V, V_{DD} =5 V	1	-		mA
Low level output current at pin INT	I_{OL2}	V_{OL} = 0.4 V, V_{DD} =5 V	1	-		mA
Low level output current at pin SDA	I_{OL3}	VOL = 0.4 V, VDD =5 V	3	-		mA
Supply low level, detected by the circuit	V_{LOW}			1	1	V

Note

1 Ta=(25 ± 5)^{o}C

2 Parameters of the quartz oscillator: f_{OSC}=32.768 kHz, R_S≤40 kOhm, C_L=8 пF

DYNAMIC CHARACTERISTICS

(T_A = –40...+ 85°C, V_{CC} = 4,5 – 5,5 V are listed in the table)

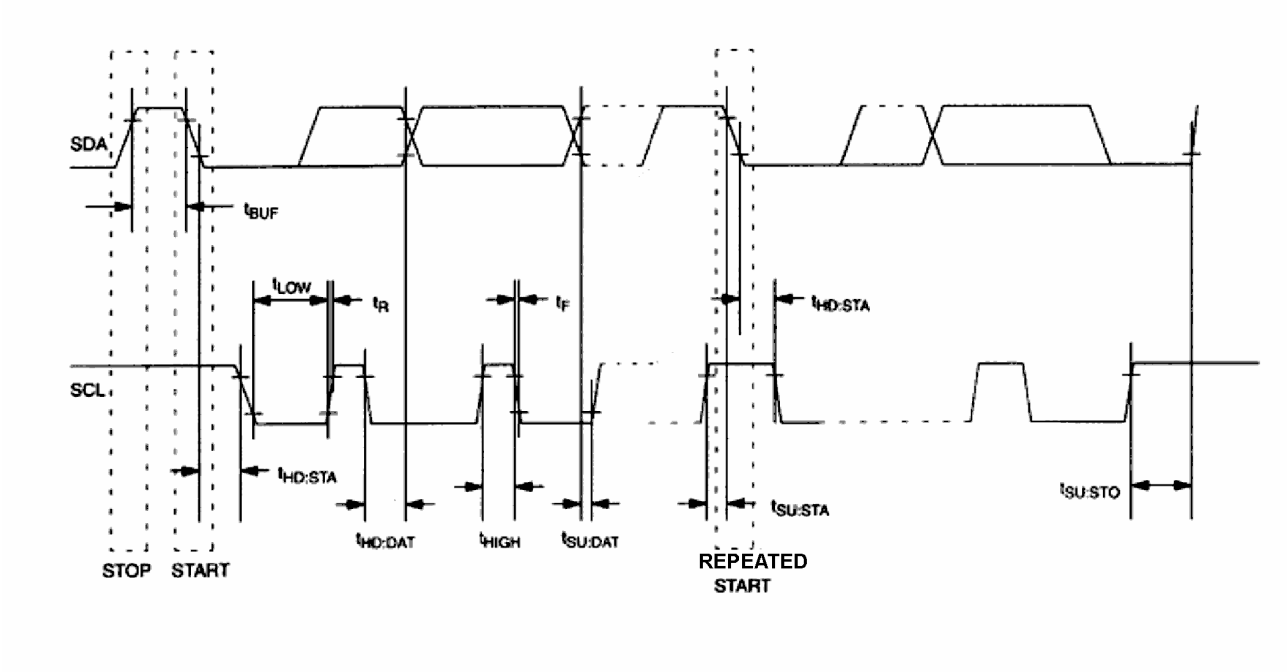
Characteristics	Symbol	Test Condition	Min	Max	Unit
Cycle frequency SCL	f_{SCL}	–	0	400	kHz
Time of bus vacant condition between the conditions STOP and START	t_{BUF}	–	4,7	–	us
Hold time (repeated) of the condition START	$t_{HD:STA}$ [1)]	–	0,6	–	us
Low condition duration of the cycle pulse SCL	t_{LOW}	–	1,3	–	us
High condition duration of the cycle pulse SCL	t_{HIGH}	–	0,6	–	us
Presetting time for the repeated condition START	$t_{SU:STA}$	–	0,6	–	us
Data hold time	$t_{HD:DAT}$ [2)]	–	0	–	us
Data presetting time	$t_{SU:DAT}$	–	100	–	ns
Rise time for signals SDA and SCL	t_R	–	–	300	ns
Drop time for signals SDA and SCL	t_F	–	–	300	ns
Presetting time for the condition STOP	$t_{SU:STO}$	–	0,6	–	us
Total capacitance load on each bus line	C_B	–	–	400	pF
Capacity input/output	$C_{I/O}$	–	10	10	pF
Load capacitance of the quartz resonator	C_{LX}	–	12,5	12,5	pF

1) After this time interval the first cycle signal is formed;

2) The device should internally ensure the hold time, at least, 300 nsec for the signal SDA (relative to V_{IHMIN} of the signal SCL) in order to overlap the indeterminancy area of the signal SCL drop front

Maximum value $t_{HD:DAT}$ should be definite in that case, if the device does not increase duration of the low condition (t_{LOW}) of the signal SCL

TIMING DIAGRAMM



OPERATION DESCRIPTION

IN1363 operates as the «slave» device on the serial bus. For access to it expedient to set the condition START and transfer after the register address the device identification code.The next registers can be address in series till the condition STOP is preset. With V_{CC} below 1,8 V, access granting to the device by the serial interface is not guaranteed. The current time is counted with the supply voltage 1 ÷ 5,5 V. When the supply level becomes lower, than 1V, the bit VL=1 is formed, signaling, that the information about the current time may be incorrect.

Description of Signals

V_{DD}– connection of the constant supply. V_{DD} – input from +1 till +5 V. With supply < 1,8 V access to the interface circuit is not guaranteed.

INT – interruption output. Interruption condition is formed with coincidence of the current time with the alarm settings, or with attainment of the condition «0» of the timer countdown. Interruption, formed from the alarm, forms the continous signal, and from the timer can be both continous and pulse one.

SCL (Input of serial synchrosignal) – SCL is used for synchronization of the dasta transfer by the serial interface.

SDA (Input/Output of serial data) – SDA is input/output for the double wire serial interface. Output SDA is the open drain, for which the external load resistor is required to be connected.

CLKOUT (Former output of the orthogonal signal) – For output activation the bit FE is preset to “1”. CLKOUT generates the orthogonal signal of four different frequencies (1 Hz, 32 Hz, 1 kHz, 32 kHz). Output CLKOUT is essentially the open drain, for which the external load resistor is required to be connected.

OSCI, OSCO – connection of the standard quartz resonator for the frequency 32,768 kHz. Capacitance load of the internal oscillator for the quartz resonator is equal to 12 pF. IN1363 can operate from the external oscillator with the frequency 32,768 kHz. With this configuration the output OSCI is connected to the signal external oscillator, and OSCO is left unconnected.

Watch and Calendar

Acquisition of information on time and date is performed by means of reading the appropriate register bytes. Presetting and time and calendar initialization is performed by means of the appropriate bytes. Information, contained in the time, calendar and alarm registers, is essentially the binary-decimal code. Bit 7 of register 2 is essentially the indication bit of the supply level decrease. < 1V (VL). When this bit = “1” , this signifies, that the supply voltage was below the norm, and the information on the current time may be unreliable.

When switching power supply on, all register bits are preset to "0", with the exception of bits FE, VL, TD1, TD0, TESTC and AE, which are preset to "1".

When applying the signal “START” on the double wire bus, the current time transfer occurs from the counters to the auxiliary set of registers. The data on time are read out from these auxiliary registers, while the watch continue to operate. This eliminates the necessity in the repeated reading in case of updating the basic registers in the access process.

Registers RTC IN1363

Address	Data								Registers / Range	
	D7	D6	D5	D4	D3	D2	D1	D0		
00H	TEST1	0	STOP	0	TESTC	0	0	0	Control 1	
01H	0	0	0	TI/TP	AF	TF	AIE	TIE	Control 2	
02H	VL	Tens of seconds			Units of seconds				Seconds	00 – 59
03H	x	Tens of minutes			Units of minutes				Minutes	00 – 59
04H	x	x	Tens of hours		Units of hours				Hours	00 – 23
05H	x	x	Tens of date		Units of date				Dates	01 – 31
06H	x	x	x	x	x	Day of week			Day of week	0 – 6
07H	C	x	x	10 M.	Units of month				Century / month	0-1/01-12
08H	Tens of years				Units of years				Year	00 – 99
09H	AE	Tens of minutes			Units of minutes				Minutes of alarm	00 – 59
0AH	AE	x	Tens of hours		Units of hours				Hours of alarm	00 – 23
0BH	AE	x	Tens of date		Units of date				Date of alarm	01 – 31
0CH	AE	x	x	x	x	Day of week			Week day of alarm	0 – 6
0DH	FE	x	x	x	x	x	FD1	FD0	Control of CLKOUT	
0EH	TE	x	x	x	x	x	TD1	TD0	Control of timer	
0FH	Value of timer								Timer	

Control Registers

Control Register 1

TEST1 (activation of test mode) – This bit, preset to logic “1”, activates the test mode, with logic “0” normal functioning of the circuit.
STOP – This bit, preset to logic “1” in the test mode perform the zero setting of all dividers, with logic “0” – normal functioning of the circuit.
TESTC (activation of the test mode) – This bit, preset to logic “1”, activates the test mode, with logic “0” normal functioning of the circuit.

Control Register 2

TI/TP (formation of the pulse interruption signal at output INT) – This bit, preset to logic “0”, with appearance of the timer flag TF at output INT forms the constant interruption signal of the low level. The bit, preset to logic “1” at output INT, forms the interruption pulse signal (signal frequencies are listed in the table).

Timer Input Frequency (Hz)	Period INT (sec).[1]	
	N =1 [2]	N > 1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1] TF and INT become active simultaneously.
[2] N – value, loaded to the timer register. Timer is stopped with N = 0.

AF (alarm flag) - bit, in logic “1” informs about interruption by actuation of the alarm, by means of software the bit AF can be reset only.
TF (timer flag) - bit, in logic “1” informs about interruption by actuation of the timer, by the software means the bit TF can be reset only.
AIE (activation of alarm) - bit, preset to logic “1”, activates operation of the alarm.
TIE (activation of timer) - bit, preset to logic “1”, activates operation of the alarm.

Control Register CLKOUT.

FE (output activation CLKOUT): This bit, preset to logic “1”, activates output CLKOUT. Frequency of the output orthogonal signal is determined by the bits FD0 and FD1.
FD – bits determine the frequency of the output orthogonal signal, when output of the orthogonal signal is activated. The frequencies are listed in the table, which can be selected by bits FD.

FD1	FD0	Frequency CLKOUT
0	0	32,768 kHz
0	1	8,192 kHz
1	0	4,096 kHz
1	1	1 Hz

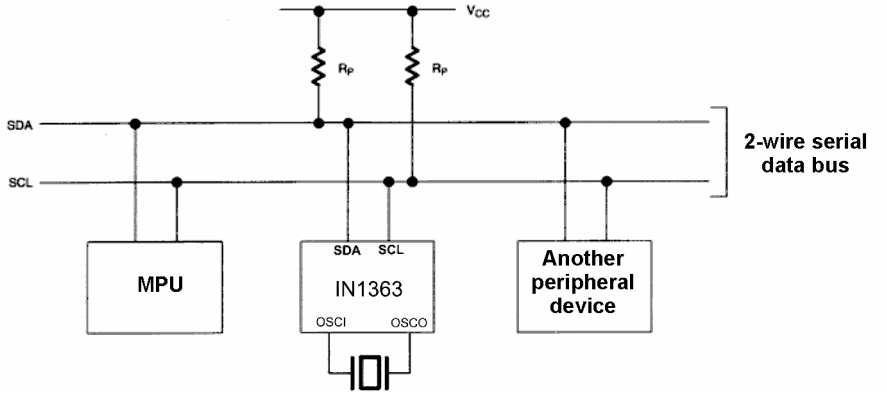
Timer Control Register

TE (timer activation): This bit, preset to logic “1”, activates the frequency application to the timer input from the oscillator. The signal frequency is determined by bits TD0 and TD1.

TD1	TD0	Timer Input Frequency
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1 / 60 Hz

Double Wire Serial Data Bus

IN1363 supports the bi-directional double wire bus and the data transfer protocol. The bus can be controlled by the “master” device, which generates the cycle signal (SCL), controls access to the bus, generates the conditions START and STOP. Typical bus configuration with the double wire is indicated in the Figure.



Data transfer can be started only when the bus is not busy. In the process of the data transfer, the data line should remain stable, while the cycle signal line is in the HIGH condition. Alterations of the data line conditions at that moment, when the cycle line is in the high condition, will be regarded as the control signals.

In compliance with this the following conditions are determined:

Bus is not busy: both lines of data and cycle signal are in the HIGH condition.

Data transfer start: Alteration of the data line condition during transition from HIGH to LOW, while the cycle line is in the HIGH condition, is determined as the status START.

Data transfer stop: Alteration of the data line condition during transition from LOW to HIGH, while the cycle line is in the HIGH condition, is determined as status STOP.

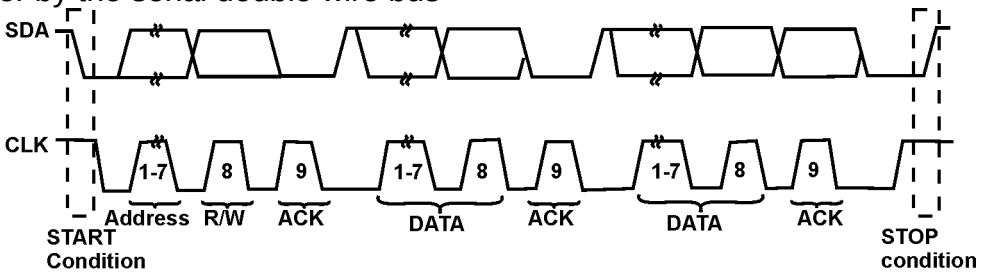
Valid data: Condition of the data line corresponds to the valid data, when after the condition START the data line is stable at the time of the HIGH status of the cycle signal. The data on the line should be altered at the time of the LOW condition of the cycle signal. One cycle pulse per one data bit.

Each data transfer starts with arrival of the status START and ceases with arrival of the status STOP. Number of data bytes, transferred between the statuses START and STOP, is not limited and is determined by the «master» device. Information is transferred byte by byte, and each reception is confirmed by the ninth bit.

Reception confirmation: Each receiving device, when being addressed, generates the reception confirmation bit after reception of each byte. The «master» device should generate the additional cycle pulses, which are set in compliance with the confirmation bits.

If the reception confirmation signal is in the high condition, then upon arrival of the confirmation cycle signal, confirming reception, the device should switch the SDA line to the low condition. Of course, the presetting time and the hold time should be taken into consideration. The «master» device should signal about termination of the data transfer to the «slave» device, stopping generation of the confirmation bit, while receiving from the «slave» cycle pulse of the reception confirmation. In this case, the «slave» cycle pulse should switch the data line to the low condition for the «master» cycle pulse to generate the condition STOP.

Data transfer by the serial double wire bus



Depending on the status of the bit $R/\overline{W}$, two types of transfer are possible:

1. Data are transferred from the «master» transmiter to the «slave» receiver. The first byte, transferred by the «master» one, is the address of the «slave» one. Then follows sequence of the data bytes. The «slave» one returns the reception confirmation bits after each received byte. Order of the data transfer: the first one is the most senior digit (MSB).

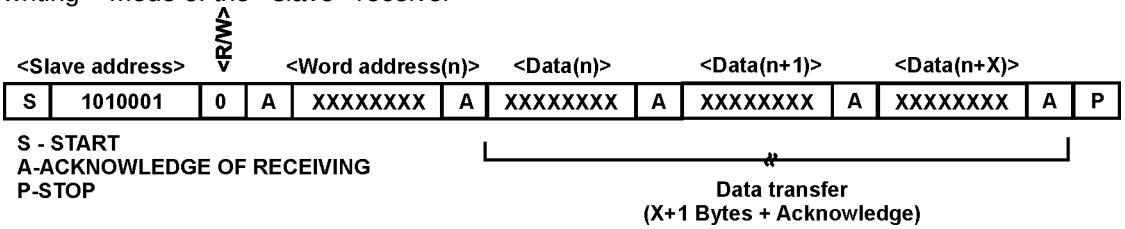
2. Data are transferred from the «slave» transmiter to the «master» receiver. The first byte (address of «slave») is transferred to the «master» one. Then the «master» returns the confirmation bit. This follows after the «slave» one of the data sequence. The «master» one returns the reception confirmation bit after each received byte, with exception of the last byte. After reception of the last byte the reception confirmation bit does not return.

The «master» device generates all cycle pulse and the conditions START and STOP. Transmission completes with emergence of the condition STOP or the repeated emergence of the condition START. As the repeated condition START is the beginning of the next serial transmission, then the bus is not vacated. Data transfer order: the first one is the most senior digit (MSB).

IC IN1363 can work in 2 next mode:

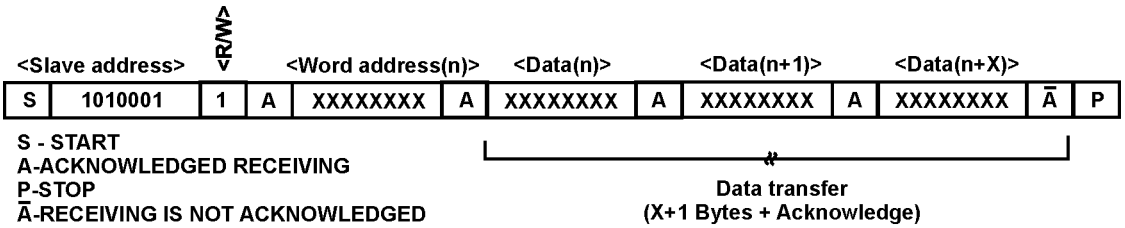
1. Mode of the «slave» receiver (writing mode of IN1363): Serial data and cycles are received via SDA and SCL appropriately. After transfer of each byte the confirming bit is transferred. Conditions START and STOP are understood as the start and end of the serial transmission. Address recognition is performed by the hardware means after reception of the address of the «slave» one and the direction bit. The address byte is the first byte, received after emergence of the condition START, generated by the «master» one. Address byte contains seven address bits IN1363, equal to 1010001, accompanied by the direction bit ($R/\overline{W}$), which is equal to 0 for writing. After reception and decoding the address IN1363 provides confirmation on the line SDA. After confirmation by IN1363 of the «slave» address and the write bit, the «master» one transmits the register address of IN1363. Thus, the register indicator will be set in IN1363. Then the «master» one will start to transfer each data byte with the subsequent confirmation reception of each byte receipt. Upon completion of writing the «master» one will form the condition STOP, for termination of the data transfer.

Data writing – mode of the «slave» receiver



2. Mode of the «slave» transmitter (read-out mode from IN1363): The first byte is accepted and is processed as in the mode of the «slave» receiver. But in this mode the direction bit will indicate, that the transmission direction is altered. The serial data are transferred by IN1363 by means of SDA, the cycle pulses – by means of SCL. The statuses of START and STOP are recognized as the start and end of transmission in series. The address byte is the first byte, received after emergence of the status START, generated by the «slave» one. The address byte contains the seven address bits DS1363, equal to 1010001, accompanied with the direction bit ($R/\overline{W}$), which is equal to 1 for reading. After reception and decoding the address byte IN1363 accepts confirmation from the line SDA. Then IN1363 starts to transmit the data from the address, to which the register indicator indicates. If the register indicator is not written prior to initialization of the writing mode, then the first read address will be the last address, stored in the register indicator. IN1363 should transmit the bit of «non-confirmation», in order to complete reading.

Data reading – mode of «slave» transmitter

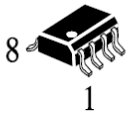


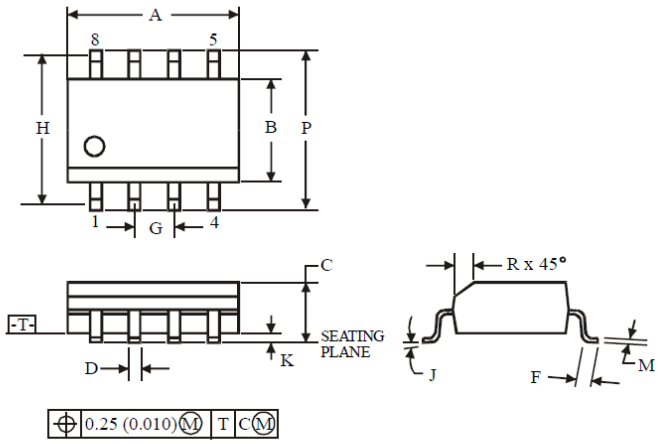
Note: last byte is followed by bit receiving is not acknowledged

PACKAGE DIMENSION

SOP 8 (MS-012AA)

D SUFFIX SOIC
(MS - 012AA)



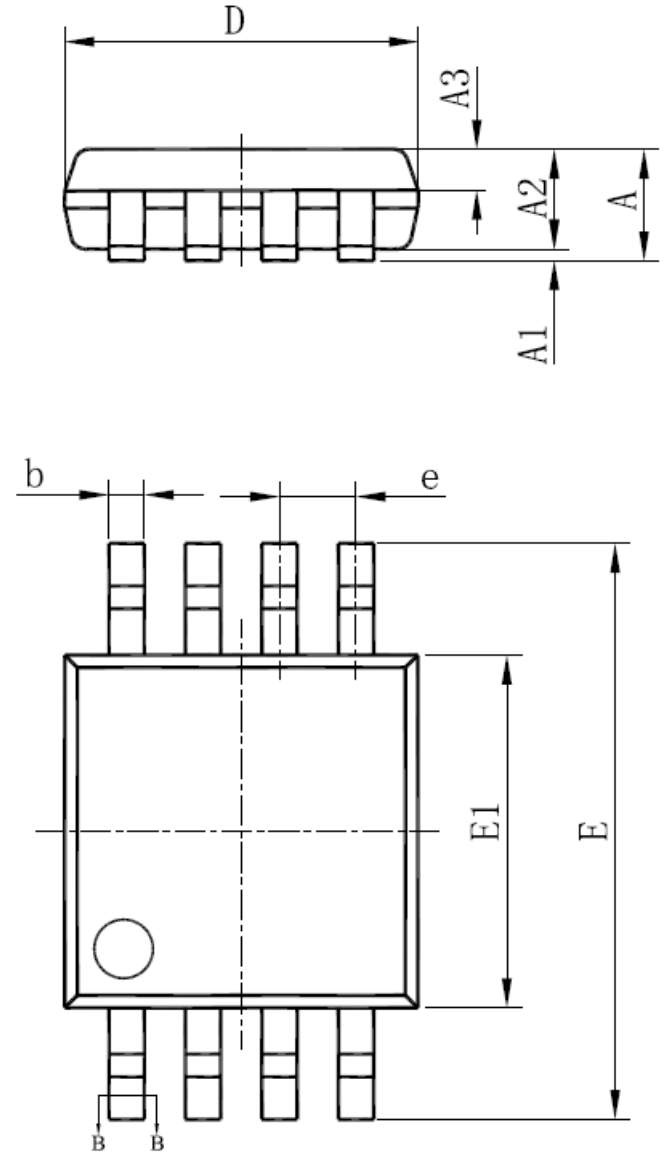


	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

MSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.29	—	0.38
b1	0.28	0.30	0.33
c	0.15	—	0.20
c1	0.14	0.152	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	71*96		