CMOSTEK

CMT2119A

240 – 960 MHz (G)FSK/OOK Transmitter

Features

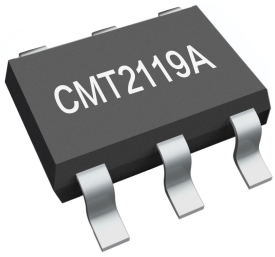
- Optional Chip Feature Configuration Schemes
  - On-Line Registers Configuration
  - Off-Line EEPROM Programming
- Frequency Range: 240 to 960 MHz
- FSK, GFSK and OOK Modulation
- Symbol Rate:
  - 0.5 to 100 ksps (FSK/GFSK)
  - 0.5 to 30 ksps (OOK)
- Deviation: 1.0 to 200 kHz
- 1-wire Interface for Transmission Control
- 2-wire Interface for Registers Accessing and EEPROM Programming
- Output Power: -10 to +13 dBm
- Supply Voltage: 1.8 to 3.6 V
- Sleep Current: < 20 nA
- FCC/ETSI Compliant
- RoHS Compliant
- 6-pin SOT23-6 Package

Applications

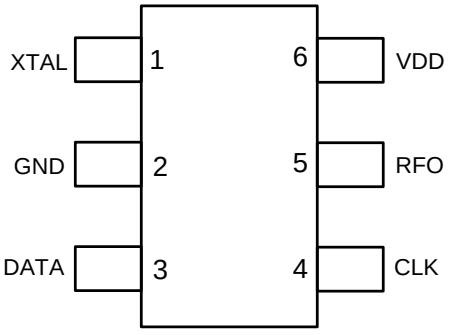
- Low-Cost Consumer Electronics Applications
- Home and Building Automation
- Remote Fan Controllers
- Infrared Transmitter Replacements
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Remote Keyless Entry (RKE)

Ordering Information

Part Number	Frequency	Package	MOQ
CMT2119A-ESR	868.35 MHz	SOT23-6	3,000 pcs
More Ordering Info: See Page 18			



SOT23-6



CMT2119A

Descriptions

The CMT2119A is a high performance, highly flexible, low-cost, single-chip (G)FSK/OOK transmitter for various 240 to 960 MHz wireless applications. It is a part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The CMT2119A provides the simplest way to control the data transmission. The transmission is started when an effective level turnover is detected on the DATA pin, while the transmission action will stop after the DATA pin holding level low for a defined time window. The chip features can be configured in two different ways: setting the configuration registers through the 2-wire interface, or programming the embedded EEPROM with CMOSTEK USB Programmer and the RFPDK. The device operates from a supply voltage of 1.8 V to 3.6 V, consumes 27.6 mA (FSK @ 868.35 MHz) when transmitting +10 dBm output power, and only leak 20 nA when it is in sleep state. The CMT2119A transmitter together with the CMT2219A receiver enables a robust RF link.

Typical Application

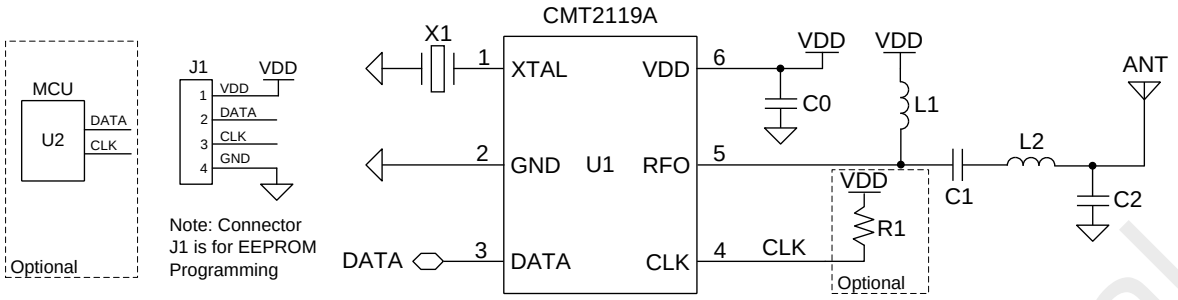


Figure 1. CMT2119A Typical Application Schematic

Table 1. BOM of 433.92/868.35 MHz Low-Cost Application

Designator	Descriptions	Value		Unit	Manufacturer
		433.92 MHz	868.35 MHz		
U1	CMT2119A, 240 – 960 MHz (G)FSK/OOK transmitter	-		-	CMOSTEK
U2	Optional MCU for on-line configuration	-		-	-
R1	Optional pull-up resistor on CLK pin	1.0		kΩ	Samsung
X1	±20 ppm, SMD32*25 mm crystal	26		MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	220	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	9	3.9	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	27	8.2	nH	Murata LQG18

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

Table of Contents

1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 868.35 MHz, FSK modulation, output power is +10 dBm terminated in a matched 50 Ω impedance, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 2. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		1.8		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

1.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 4. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		960	MHz
Synthesizer Frequency Resolution	F_{RES}	F_{RF} < 500 MHz		198		Hz
		F_{RF} > 500 MHz		397		Hz
Symbol Rate	SR	FSK/GFSK	0.5		100	ksps
		OOK	0.5		30	ksps
(G)FSK Modulation Deviation Range	F_{DEV}		1		200	kHz
Bandwidth-Time Product	BT	GFSK modulation	-	0.5	-	-
Maximum Output Power	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
OOK PA Ramping Time[2]	t_{RAMP}		0		1024	us
Current Consumption @ 433.92 MHz	$I_{DD-433.92}$	OOK, 0 dBm, 50% duty cycle		6.7		mA
		OOK, +10 dBm, 50% duty cycle		13.4		mA
		OOK, +13 dBm, 50% duty cycle		17.4		mA
		FSK, 0 dBm, 9.6 ksps		10.5		mA
		FSK, +10 dBm, 9.6 ksps		23.5		mA
		FSK, +13 dBm, 9.6 ksps		32.5		mA
Current Consumption @ 868.35 MHz	$I_{DD-868.35}$	OOK, 0 dBm, 50% duty cycle		8.0		mA
		OOK, +10 dBm, 50% duty cycle		15.5		mA
		OOK, +13 dBm, 50% duty cycle		19.9		mA
		FSK, 0 dBm, 9.6 ksps		12.3		mA
		FSK, +10 dBm, 9.6 ksps		27.6		mA
		FSK, +13 dBm, 9.6 ksps		36.1		mA
Sleep Current	I_{SLEEP}			20		nA
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @ 433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Phase Noise @ 868.35 MHz	$PN_{868.35}$	100 kHz offset from F_{RF}		-74		dBc/Hz
		600 kHz offset from F_{RF}		-92		dBc/Hz
		1.2 MHz offset from F_{RF}		-101		dBc/Hz
Harmonics Output for 433.92 MHz[3]	$H2_{433.92}$	2^{nd} harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3^{rd} harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
Harmonics Output for 868.35 MHz [3]	$H2_{868.35}$	2^{nd} harm @ 1736.7 MHz, +13 dBm P_{OUT}		-67		dBm
	$H3_{868.35}$	3^{rd} harm @ 2605.05 MHz, +13 dBm P_{OUT}		-55		dBm
OOK Extinction Ration				60		dB

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. 0 and 2^n us, n = 0 to 10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

[3]. The harmonics output is measured with the application shown as Figure 10.

1.4 Crystal Oscillator

Table 5. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}		12		20	pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The CMT2119A can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

2. Pin Descriptions

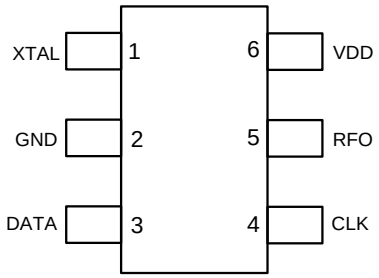


Figure 2. CMT2119A Pin Assignments

Table 6. CMT2119A Pin Descriptions

Pin Number	Name	I/O	Descriptions
1	XTAL	I	26 MHz single-ended crystal oscillator input or External 26 MHz reference clock input
2	GND	I	Ground
3	DATA	IO	Data input to be transmitted or Data pin to access the embedded EEPROM
4	CLK	I	Clock pin to access the embedded EEPROM
5	RFO	O	Power amplifier output
6	VDD	I	Power supply input

3. Typical Performance Characteristics

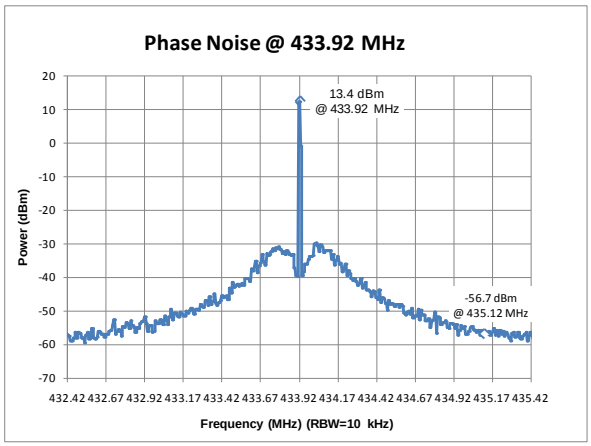


Figure 3. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

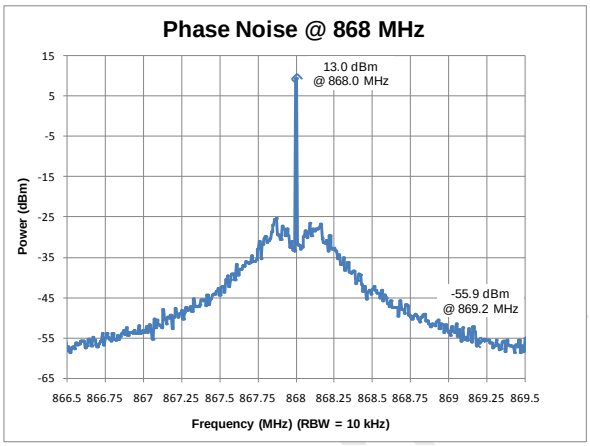


Figure 4. Phase Noise, F_{RF} = 868 MHz, P_{OUT} = +13 dBm, Unmodulated

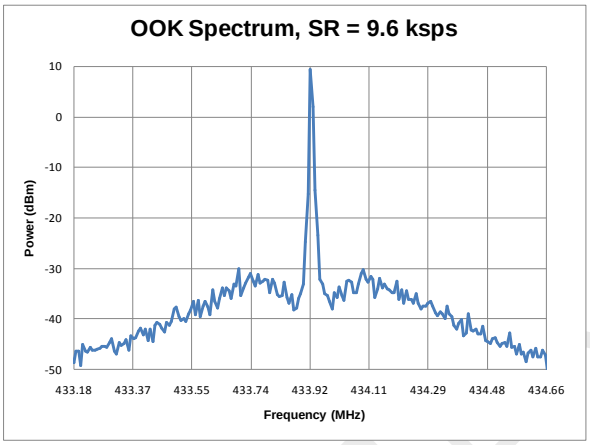


Figure 5. OOK Spectrum, SR = 9.6 ksps, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

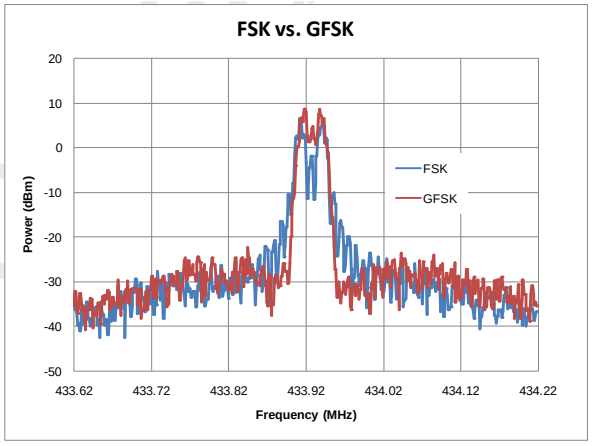


Figure 6. FSK/GFSK Spectrum, SR = 9.6 ksps, F_{DEV} = 15 kHz

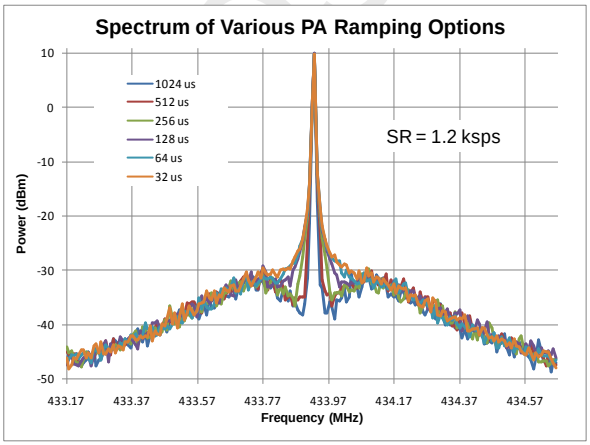


Figure 7. Spectrum of PA Ramping, SR = 1.2 ksps, P_{OUT} = +10 dBm

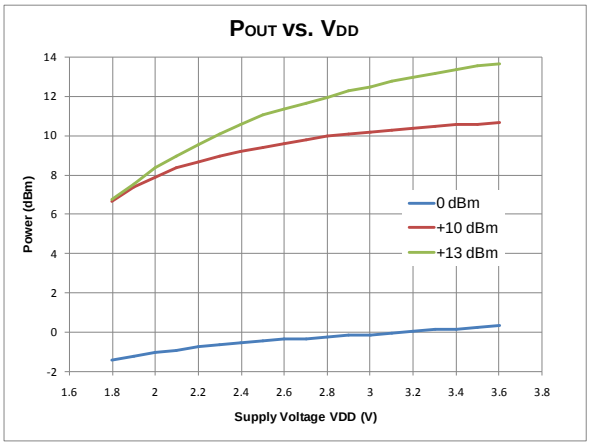


Figure 8. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

4. Typical Application Schematics

4.1 Low-Cost Application Schematic

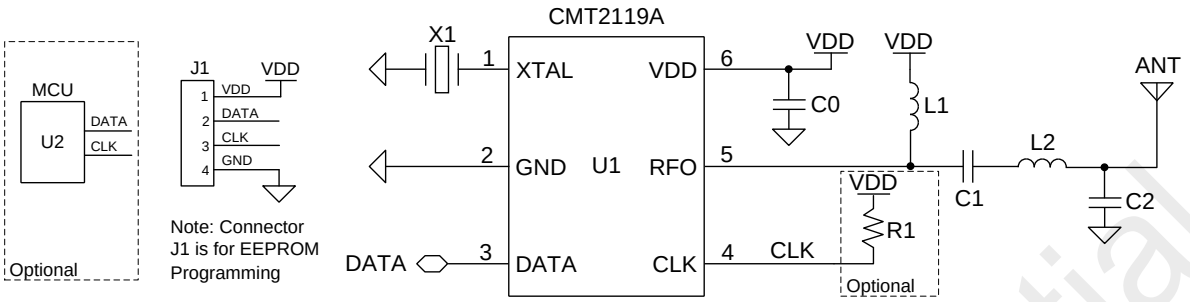


Figure 9. Low-Cost Application Schematic

Notes:

1. Connector J1 is a must for the CMT2119A EEPROM access during development or manufacture.
2. An external MCU U2 is necessary if on-line register configuration is required.
3. A 1.0 kΩ pull-up resistor R1 is recommended to enhance the robustness of the chip. If the driving source for the EEPROM programming is not strong enough, the R1 should be removed during the EEPROM Programming.
4. The general layout guidelines are listed below. For more design details, please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline"
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2119A as possible for better filtering.
5. The table below shows the BOM of 433.92/868.35 MHz Low-Cost Applications. For the BOM of 315/915 MHz application, please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline".

Table 7. BOM of 433.92/868.35 MHz Low-Cost Application

Designator	Descriptions	Value		Unit	Manufacturer
		433.92 MHz	868.35 MHz		
U1	CMT2119A, 240 – 960 MHz (G)FSK/OOK transmitter	-		-	CMOSTEK
U2	Optional MCU for on-line configuration	-		-	-
R1	Optional pull-up resistor on CLK pin	1.0		kΩ	Samsung
X1	±20 ppm, SMD32*25 mm crystal	26		MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	220	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	9	3.9	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	27	8.2	nH	Murata LQG18

4.2 FCC/ETSI Compliant Application Schematic

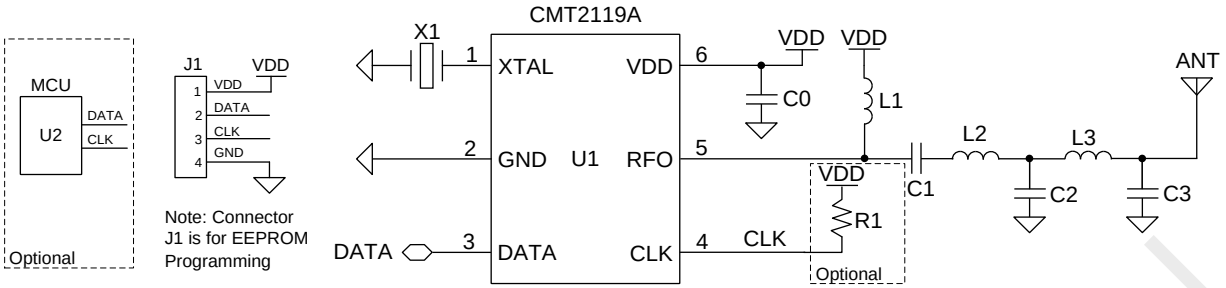


Figure 10. FCC/ETSI Compliant Application Schematic

Notes:

1. Connector J1 is a must for the CMT2119A EEPROM access during development or manufacture.
2. An external MCU U2 is necessary if on-line register configuration is required.
3. A 1.0 kΩ pull-up resistor R1 is recommended to enhance the robustness of the chip. If the driving source for the EEPROM programming is not strong enough, the R1 should be removed during the EEPROM Programming.
4. The general layout guidelines are listed below. For more design details, please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline".
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2119A as possible for better filtering.
5. The table below shows the BOM of 433.92/868.35 MHz FCC/ETSI Compliant Application. For the BOM of 315 and 915 MHz application, please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline".

Table 8. BOM of 433.92/868.35 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value		Unit	Manufacturer
		433.92 MHz	868.35 MHz		
U1	CMT2119A, 240 – 960 MHz (G)FSK/OOK transmitter	-		-	CMOSTEK
U2	Optional MCU for on-line configuration	-		-	-
R1	Optional pull-up resistor on CLK pin	1.0		kΩ	Samsung
X1	±20 ppm, SMD32*25 mm crystal	26		MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	15	9.1	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	15	8.2	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	36	8.2	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	18	8.2	nH	Murata LQG18

5. Functional Descriptions

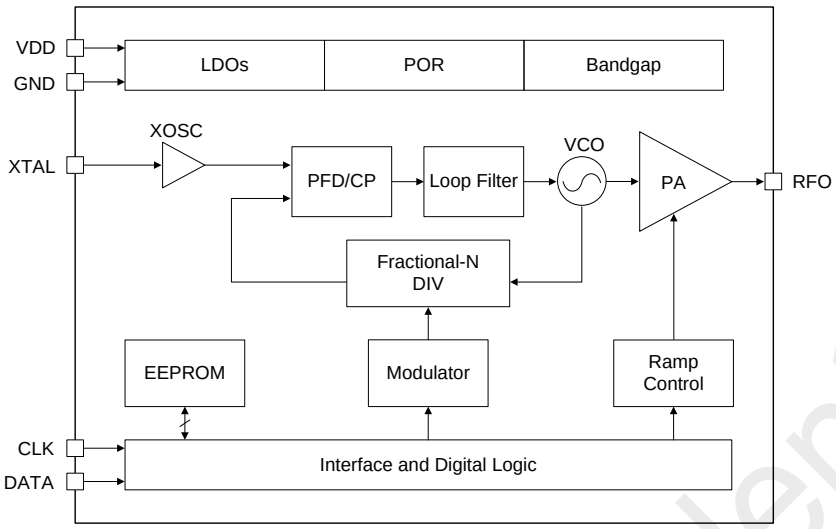


Figure 11. CMT2119A Functional Block Diagram

5.1 Overview

The CMT2119A is a high performance, highly flexible, low-cost, single-chip (G)FSK/OOK transmitter for various 240 to 960 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2119A is shown in the figure above. The CMT2119A is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the internal voltage reference. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2119A requires only 1 wire for the external MCU or encoder to send in the data and control the transmission. The input data will be modulated and sent out by a highly efficient PA which output power can be configured from -10 to +13 dBm in 1 dB step size.

The user can directly use the CMT2119A default configuration for immediate demands. If that cannot meet the system requirement, on-line register configuration and off-line EEPROM programming configuration are available for the user to customize the chip features. The on-line configuration means there is an MCU available in the application to configure the chip registers through the 2-wire interface, while the off-line configuration is done by the CMOSTEK USB Programmer and the RFPDK. After the configuration is done, only 1-wire interface is required for the external MCU or encoder to send in the data and control the transmission The CMT2119A operates from 1.8 to 3.6 V so that it can finely work with most batteries to their useful power limits. It only consumes 15.5 mA (OOK @ 868.35 MHz) / 27.6 mA (FSK @ 868.35 MHz) when transmitting +10 dBm power under 3.3 V supply voltage.

5.2 Modulation, Frequency, Deviation and Symbol Rate

The CMT2119A supports GFSK/FSK modulation with the symbol rate up to 100 ksps, as well as OOK modulation with the symbol rate up to 30 ksps. The supported deviation of the (G)FSK modulation ranges from 1 to 200 kHz. The CMT2119A continuously covers the frequency range from 240 to 960 MHz, including the license free ISM frequency band around 315 MHz, 433.92 MHz, 868.35 MHz and 915 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz when the frequency is less than 500 MHz, and is about 397 Hz

when the frequency is larger than 500 MHz. See the table below for the modulation, frequency and symbol rate specifications.

Table 9. Modulation, Frequency and Symbol Rate

Parameter	Value	Unit
Modulation	(G)FSK/OOK	-
Frequency	240 to 960	MHz
Deviation	1 to 200	kHz
Frequency Resolution (F_{RF} < 500 MHz)	198	Hz
Frequency Resolution (F_{RF} > 500 MHz)	397	Hz
Symbol Rate (FSK/GFSK)	0.5 to 100	ksps
Symbol Rate (OOK)	0.5 to 30	ksps

5.3 Embedded EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the CMT2119A in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. No register access and control is required in the application program. See the figure below for the accessing of the EEPROM and Table 10 for the summary of all the configurable parameters of the CMT2119A in the RFPDK.

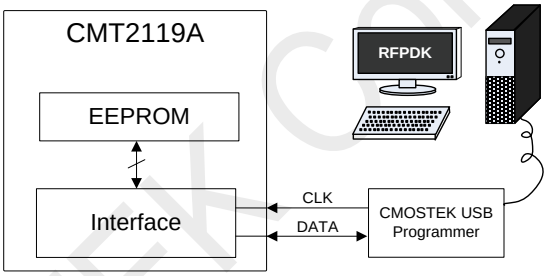


Figure 12. Accessing Embedded EEPROM

For more details of the CMOSTEK USB Programmer and the RFPDK, please refer to "AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide". For the detail of CMT2119A configurations with the RFPDK, please refer to "AN122 CMT2119A Configuration Guideline".

Table 10. Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency	To input a desired transmitting radio frequency in the range from 240 to 960 MHz. The step size is 0.01 MHz.	868.35 MHz	Basic Advanced
	Modulation	The option is FSK or GFSK and OOK.	FSK	Basic Advanced
	Deviation	The FSK frequency deviation. The range is from 1 to 100 kHz.	35 kHz	Basic Advanced
	Symbol Rate	The GFSK symbol rate. The user does not need to specified symbol rate for FSK and OOK modulation.	2.4 ksps	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dB margin is given above +13 dBm.	+13 dBm	Basic Advanced
	Xtal Load	On-chip XOSC load capacitance options: from 10 to 22 pF. The step size is 0.33 pF.	15 pF	Basic Advanced
	Data Representation	To select whether the frequency “Fo + Fdev” represent data 0 or 1. The options are: 0: F-high 1: F-low, or 0: F-low 1: F-high.	0: F-low 1: F-high	Advanced
	PA Ramping	To control PA output power ramp up/down time for OOK transmission, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising/Falling Edge.	Data Pin Rising Edge	Advanced
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 2 to 90 ms.	Data Pin Holding Low for 2 ms	Advanced

5.4 On-line Configuration

The on-line configuration means there is an MCU available in the application to configure the chip registers through the 2-wire interface (CLK and DATA). The value of the registers, which is originally copied from the EEPROM at the chip’s power-up, will remain its value until part or all of the registers are modified by the external MCU. The register value will be lost after the chip's power-down, and re-configuration is necessary when it is powered up again.

Please note that the DATA pin is the only pin required by the transmission control, and it is also reused as the data port of the 2-wire interface for register access and EEPROM programming. For the detail of the register configuration, please refer to “AN122 CMT2119A Configuration Guideline”.

5.5 Power Amplifier

A highly efficient single-ended Power Amplifier (PA) is integrated in the CMT2119A to transmit the modulated signal out. Depending on the application, the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application Schematic”. For the schematic, layout guideline and the other detailed information please refer to “AN101 CMT211xA Schematic and PCB Layout Design Guideline”.

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and RFPDK.

5.6 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The CMT2119A has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 13. These options are only available when the modulation type is OOK. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below.

$$SR_{Max} \leq 0.5 * (\frac{1}{t_{RAMP}})$$

In which the PA ramping “rate” is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by formula below.

$$t_{RAMP} \leq 0.5 * (\frac{1}{SR_{MAX}})$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than “$0.5 * (1/SR_{Max})$”, it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to “AN122 CMT2113/19A Configuration Guideline”.

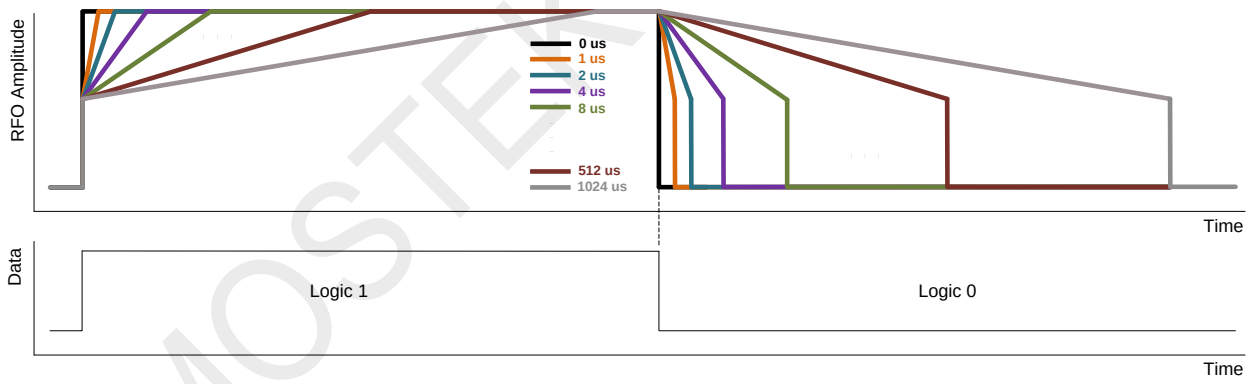


Figure 13. PA Ramping Time

5.7 Working States and Control Interface

The CMT2119A has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2119A is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized to 20 nA typically. The interface is ready to sense a valid rising or falling edge on DATA pin to start a transmitting cycle.

XO-STARTUP

After the CMT2119A received the valid control signal, it will go into the XO-STARTUP state, and the internal XO starts to work. The user has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table 11.

TUNE

The frequency synthesizer will tune the CMT2119A to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the incoming data only after the TUNE state is done, before that the incoming data will not be transmitted.

TRANSMIT

The CMT2119A starts to modulate and transmit the data coming from the DATA pin. After the DATA pin is driven to low for the time t_{STOP} (can be configured from 20 to 90 ms in 10 ms step size through the RFPDK), the transmission will be ended and the CMT2119A will go back to the SLEEP state, waiting for the next transmitting cycle.

The transmission can be enabled by either “DATA Pin Rising Edge” or “DATA Pin Falling Edge”. See the Table 11, Figure 14 and Figure 15 for the timing requirement of each working state in the 2 different modes.

Table 11.Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop the Transmission[2]	t_{STOP}	2		90	ms

Notes:
[1]. This parameter is to a large degree crystal dependent.
[2]. Configurable from 2 to 9 in 1 ms step size and 20 to 90 ms in 10 ms step size.

5.7.1 Tx Enabled by DATA Pin Rising Edge

As shown in the figure below, once the CMT2119A detects a rising edge on the DATA pin, it goes into the XO-STARTUP state. The user has to pull the DATA pin high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the DATA pin. The logic state of the DATA pin is “don't' care” from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission.

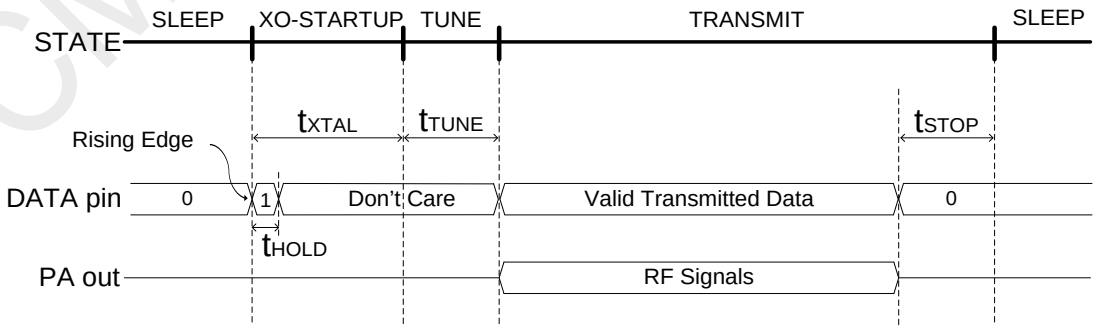


Figure 14. Transmission Enabled by DATA Pin Rising Edge

5.7.2 Tx Enabled by DATA Pin Falling Edge

As shown in the figure below, once the CMT2119A detects a falling edge on the DATA pin, it goes into XO-STARTUP state and the XO starts to work. During the XO-STARTUP state, the DATA pin needs to be pulled low. After the XO is settled, the CMT2119A goes to the TUNE state. The logic state of the DATA pin is “don't’ care” during the TUNE state. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission. Before starting the next transmit cycle, the user has to pull the DATA pin back to high.

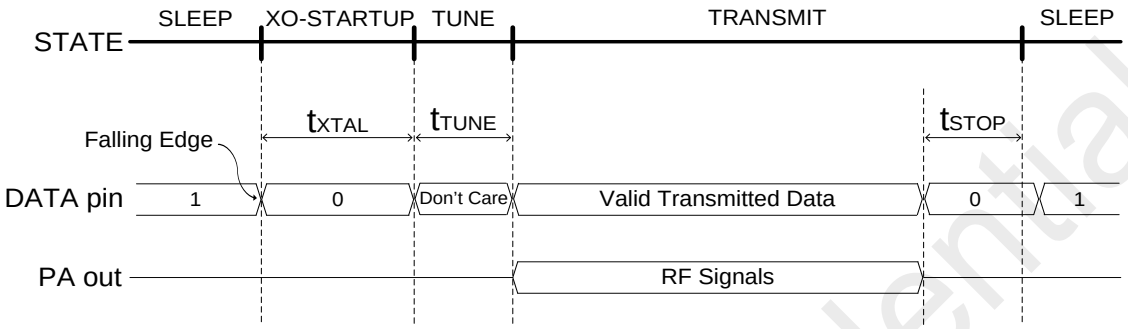


Figure 15. Transmission Enabled by DATA Pin Falling Edge

5.8 Crystal Oscillator and RCLK

The CMT2119A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 16 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the CMT2119A to support the oscillation of the crystal.

The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency. Please refer to “AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide” for the method of choosing the right value of C_L.

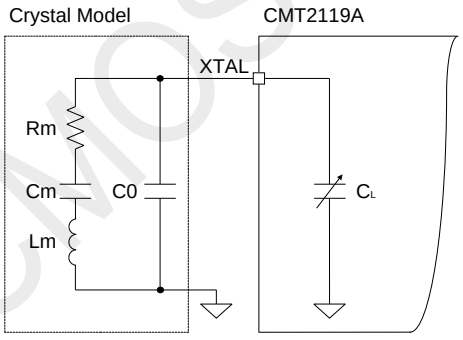


Figure 16. XTAL Circuitry and Crystal Model

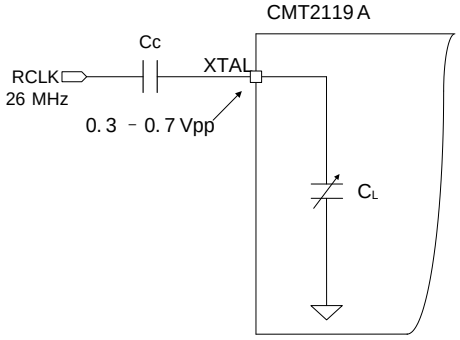


Figure 17. RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2119A by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 17 for the RCLK circuitry.

6. Ordering Information

Table 12. CMT2119A Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2119A-ESR[1]	240-960 MHz (G)FSK/OOK Transmitter	SOT23-6	Tape & Reel	1.8 to 3.6 V, -40 to 85 ℃	3,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.
"S" stands for the package type of SOT23-6 for this product.
"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 3,000 pieces.

Visit www.cmostek.com/products to know more about the product and product line.
Contact sales@cmostek.com or your local sales representatives for more information.

7. Package Outline

The 6-pin SOT23-6 illustrates the package details for the CMT2119A. The table below lists the values for the dimensions shown in the illustration.

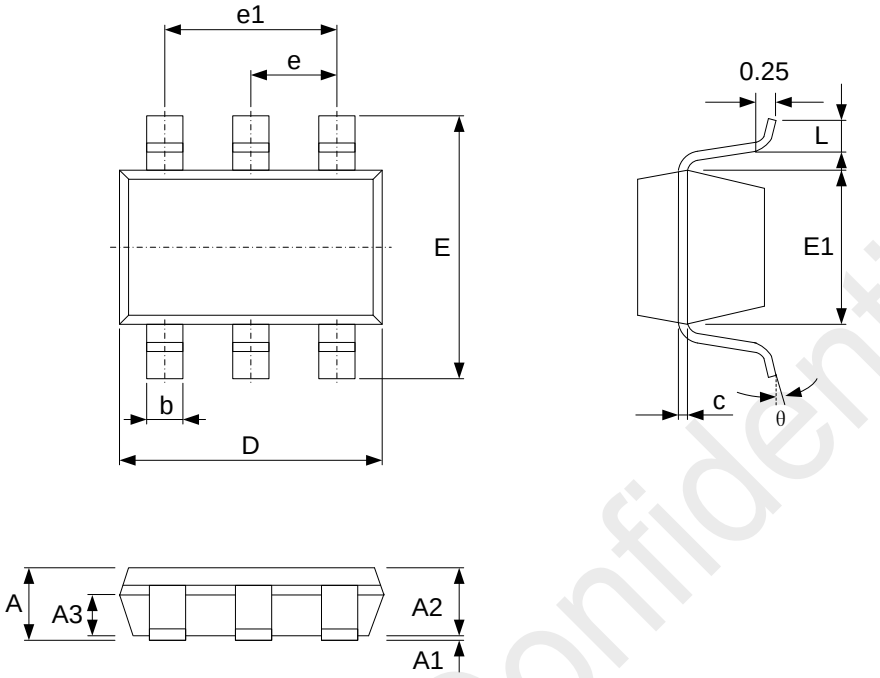


Figure 18. 6-Pin SOT23-6

Table 13. 6-Pin SOT23-6 Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	—	—	1.35
A1	0.04	—	0.15
A2	1.00	1.10	1.20
A3	0.55	0.65	0.75
b	0.38	—	0.48
C	0.08	—	0.20
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	—	0.60
θ	0	—	8°

8. Top Marking

8.1 CMT2119A Top Marking

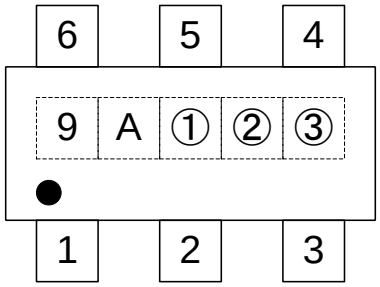


Figure 19. CMT2119A Top Marking

Table 14. CMT2119A Top Marking Explanation

Top Mark	9A①②③
Mark Method	Laser
Font Size	0.6 mm, right-justified
1st letter	9, represents CMT2119
2nd letter	A: represents revision A
3rd – 5th letter	①②③: Internal reference for data code tracking, assigned by the assembly house

9. Other Documentations

Table 15. Other Documentations for CMT2119A

Brief	Name	Descriptions
AN101	CMT211xA Schematic and PCB Layout Design Guideline	Details of CMT211xA PCB schematic and layout design rules, RF matching network and other application layout design related issues.
AN122	CMT2119A Configuration Guideline	Details of configuring CMT2119A features on the RFPDK, and the on-line configuration guideline for CMT2119A.
AN103	CMT211xA-221xA One-Way RF Link Development Kits Users Guide	User's Guides for CMT211xA/CMT221xA Development Kits, including Evaluation Board and Evaluation Module, CMOSTEK USB Programmer and RFPDK.

10. Document Change List

Table 16. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.6	All	Initial Released	2014-12-05

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