Low-Noise Programmable Linear Hall Effect Sensor ICs with Adjustable Bandwidth (50 kHz Maximum) and Analog Output

Features and Benefits

- 1 mm case thickness provides greater coupling for current sensing applications
- Customer programmable offset and sensitivity
- Factory programmed 0%/°C sensitivity temperature coefficient
- Programmability at end-of-line
- Selectable unipolar or bipolar quiescent voltage levels
- Selectable sensitivity ranges between 0.7 and 1.4 mV/G (A1360), 1.4 to 4.5 mV/G (A1361) and 4.5 to 16 mV/G (A1362)
- Device bandwidth selectable under 50 kHz, via capacitor on FILTER pin
- Ratiometric sensitivity, quiescent voltage output, and clamps for interfacing with application DAC
- Temperature-stable quiescent voltage output and sensitivity
- Precise recoverability after temperature cycling
- Output voltage clamps provide short circuit diagnostic capabilities
- Wide ambient temperature range: – 40°C to 150°C
- Resistant to mechanical stress

Package: 4 pin SIP (suffix KT)

Description

New applications for linear output Hall effect sensing, such as current measurement, require both high accuracy and increased sensor bandwidth. The Allegro® A1360, A1361, and A1362 programmable linear Hall effect sensor ICs are designed specifically to achieve both goals. Available in a through-hole SIP (single in-line package), the A136x Hall effect sensor ICs are sensitive and temperature-stable. The accuracy of these devices is enhanced via programmability on the device VOUT pin. A capacitor to ground on the FILTER pin on the A136x can be used to tune the device bandwidth in a range less than 50 kHz.

These ratiometric Hall effect sensor ICs provide a voltage output that is proportional to the applied magnetic field. The quiescent output voltage is user-adjustable around either 50% (bidirectional configuration) or 10% (unidirectional configuration) of the supply voltage, V_{CC}. The device sensitivity is adjustable within three guaranteed ranges: 0.7 to 1.4 mV/G (A1360), 1.4 to 4.5 mV/G (A1361), and 4.5 to 16 mV/G (A1362).

Each BiCMOS monolithic circuit integrates a Hall element, temperature-compensation circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary dynamic offset cancellation technique.

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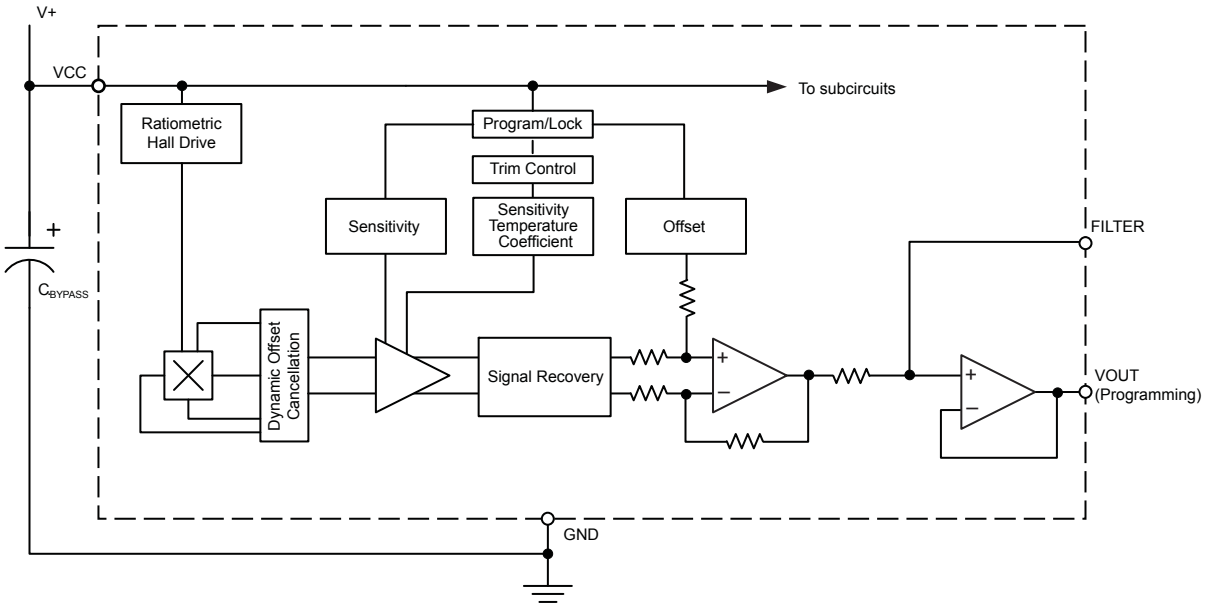
Functional Block Diagram



Description (continued)

The features of these linear Hall effect sensor ICs make them ideal for meeting high accuracy requirements in automotive and industrial applications. Device specifications are guaranteed over an extended ambient temperature range: –40 °C to 150 °C. The A136x sensor ICs are provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT) that is lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide[1]

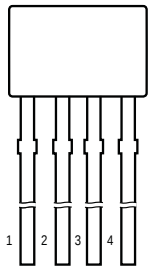
Part Number	Packing[2]	Sensitivity Range (mV/G)
A1360LKTTN-T	4000 pieces per 13-in. reel	0.7 to 1.4
A1361LKTTN-T	4000 pieces per 13-in. reel	1.4 to 4.5
A1362LKTTN-T	4000 pieces per 13-in. reel	4.5 to 16

[1]All variants are programmable for unidirectional or bidirectional use.
[2]Contact Allegro for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		28	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Forward Filter Voltage	V_{FILTER}		8	V
Reverse Filter Voltage	$V_{RFILTER}$		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	3	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	10	mA
Ambient Operating Temperature	T_A	Range L	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Junction Temperature	T_J(max)		165	°C

Pin-out Diagram



Terminal List Table

Number	Name	Description
1	VCC	Input power supply; use bypass capacitor to connect to ground
2	VOUT	Output signal; also used for programming
3	FILTER	Terminal for external filter capacitor for bandwidth setting
4	GND	Ground

OPERATING CHARACTERISTICS valid over full operating temperature range, T_A; C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Electrical Characteristics						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	No load on VOUT	–	9.2	12	mA
Power-On Time[1]	t_{PO}	T_A = 25°C, C_L (of test probe) = 10 pF, C_{BYPASS} = open; Sens = 4.5 mV/G	–	30	–	µs
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, I_{CC} = 13 mA	6	7.6	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, 100 $G_{(P-P)}$ magnetic input signal, C_{FILTER} = open, C_L = 10 nF	50	–	–	kHz
Filtered Bandwidth	BW_f	Small signal –3 dB, 100 $G_{(P-P)}$ magnetic input signal, C_{FILTER} = 1 nF, C_L = 10 nF	–	–	50	kHz
Chopping Frequency[2]	f_C	T_A = 25°C	–	210	–	kHz
Output Characteristics						
Propagation Delay Time[1]	t_{pd}	T_A = 25°C, impulse magnetic field of 400 G, C_{FILTER} = open, C_L = 10 nF	–	1.6	–	µs
Rise Time[1]	t_r	T_A = 25°C, impulse magnetic field of 400 G, C_{FILTER} = open, C_L = 10 nF	–	5.5	–	µs
Response Time[1]	$t_{RESPONSE}$	T_A = 25°C, C_L = 10 nF	–	7.0	–	µs
Delay to Clamp[1]	t_{CLP}	T_A = 25°C, impulse magnetic field of 400 G, C_{FILTER} = open, C_L = 10 nF	–	30	–	µs
Output Voltage Clamp[3]	$V_{CLP(HIGH)}$	A1360	T_A = 25°C, B = 600 G, Sens = 5.0 mV/G, $R_{L(PULLDWN)}$ = 10 kΩ	4.65	4.73	4.80	V
		A1361		4.65	4.73	4.80	V
		A1362		4.65	4.78	4.91	V
	$V_{CLP(LOW)}$	A1360	T_A = 25°C, B = 600 G, Sens = 5.0 mV/G, $R_{L(PULLUP)}$ = 10 kΩ	0.25	0.32	0.4	V
		A1361		0.25	0.32	0.4	V
		A1362		0.25	0.32	0.4	V
Noise (peak-to-peak)[4]	$V_{N(p-p)}$	T_A = 25°C, C_L = 10 nF, Sens = 1.5 mV/G, C_{FILTER} = 1 nF (BW_f = 50 kHz)	–	8	–	mV
		T_A = 25°C, C_L = 10 nF, Sens = 6.6 mV/G, C_{FILTER} = 47 nF (BW_f = 2 kHz)	–	8.5	–	mV
		T_A = 25°C, C_L = 10 nF, Sens = 6.6 mV/G, C_{FILTER} = 1 nF (BW_f = 50 kHz)	–	38	–	mV
DC Output Resistance	R_{OUT}		–	<1	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L\ (PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	–	10	nF
Phase Shift[5]	ΔΦ	C_L = 10 nF, C_{FLITER} = 1 nF (BW = 50 kHz), magnetic input signal frequency = 1 kHz with 1 $V_{(p-p)}$ output signal	–	2.5	–	deg.
Output Slew Rate[6]	SR	Sens = 4.5 mV/G, C_L = 10 nF	–	210	–	V/ms

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OPERATING CHARACTERISTICS (continued) valid over full operating temperature range, T_A; C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Pre-Programming Target[7]						
Pre-Programming Quiescent Voltage Output	$V_{OUT(Q)PRE}$	B = 0 G, T_A = 25°C	–	2.0	–	V
Pre-Programming Sensitivity	$Sens_{PRE}$	A1360, T_A = 25°C	–	0.5	–	mV/G
		A1361, T_A = 25°C	–	1.1	–	mV/G
		A1362, T_A = 25°C	–	2.7	–	mV/G
Quiescent Voltage Output Programming						
Initial Quiescent Voltage Output[8]	$V_{OUT(Q)UNIinit}$	B = 0 G, T_A = 25°C	–	$V_{CLP(LOW)}$	–	V
	$V_{OUT(Q)BIinit}$	B = 0 G, T_A = 25°C	–	$V_{OUT(Q)PRE}$	–	V
Coarse Quiescent Voltage Output Programming Bits[9]			–	1	–	bit
Guaranteed Quiescent Voltage Output Range[10,11]	$V_{OUT(Q)UNI}$	B = 0 G, T_A = 25°C	0.40	–	1.15	V
	$V_{OUT(Q)BI}$	B = 0 G, T_A = 25°C	2.15	–	2.85	V
Quiescent Voltage Output Programming Bits			–	8	–	bit
Average Quiescent Voltage Output Step Size[12,13]	$Step_{VOUT(Q)}$	T_A = 25°C	3.4	3.85	4.4	mV
Quiescent Output Voltage Programming Resolution[14]	$Err_{PGVOUT(Q)}$	T_A = 25°C	–	$Step_{VOUT(Q)}$ × ±0.5	–	mV
Sensitivity Programming						
Initial Sensitivity	$Sens_{init}$	T_A = 25°C	–	$Sens_{PRE}$	–	mV/G
Guaranteed Sensitivity Range[15,16]	Sens	A1360, T_A = 25°C	0.7	–	1.4	mV/G
		A1361, T_A = 25°C	1.4	–	4.5	mV/G
		A1362, T_A = 25°C	4.5	–	16	mV/G
Sensitivity Programming Bits			–	8	–	bit
Average Sensitivity Step Size[12,13]	$Step_{SENS}$	A1360, T_A = 25°C	4.2	5.3	6.2	µV/G
		A1361, T_A = 25°C	15	16	21	µV/G
		A1362, T_A = 25°C	65	79	90	µV/G
Sensitivity Programming Resolution[14]	Err_{PGSENS}	T_A = 25°C	–	$Step_{SENS}$ × ±0.5	–	µV/G
Lock Bit Programming						
Overall Programming Lock Bit	LOCK		–	1	–	bit
Factory-Programmed Sensitivity Temperature Coefficient						
Sensitivity Temperature Coefficient[17]	TC_{SENS}		–0.025	0	0.025	%/°C
Error Components						
Linearity Sensitivity Error[18]	Lin_{ERR}	A1360	–3.0	–	3.0	%
		A1361	–2.5	–	2.5	%
		A1362	–2.0	–	2.0	%
Symmetry Sensitivity Error[19]	Sym_{ERR}	A1360	–3.5	–	3.5	%
		A1361	–3.0	–	3.0	%
		A1362	–3.0	–	3.0	%
Ratiometry Quiescent Voltage Output Error[20]	$Rat_{ERRVOUT(Q)}$		–	< ±1.5	–	%
Ratiometry Sensitivity Error[20]	$Rat_{ERRSENS}$		–	< ±1.5	–	%
Ratiometry Clamp Error[21]	$Rat_{SENSCLP}$	T_A = 25°C	–	< ±1.5	–	%

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OPERATING CHARACTERISTICS (continued) valid over full operating temperature range, T_A; C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Drift Characteristics							
Quiescent Voltage Output Drift Through Temperature Range[1]	$\Delta V_{OUT(Q)}$	A1360	$V_{OUT(Q)}$ = 2.5 V; Sens = Sens(min)	–20	–	20	mV
		A1361		–20	–	20	mV
		A1362		–60	–	60	mV
		A1360	$V_{OUT(Q)}$ = 2.5 V; Sens = Sens(max)	– 35	–	35	mV
		A1361		–50	–	50	mV
		A1362		–160	–	160	mV
Sensitivity Drift Due to Package Hysteresis[1]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling		–	< ±1	–	%

[1] See Characteristic Definitions section.

[2] f_C varies up to approximately ±20% over the full operating ambient temperature range, T_A, and process.

[3] V_{CLP} voltages are production-tested, with the sole exception of the A1360 $V_{CLP(HIGH)}$, which is guaranteed by design (the low sensitivity and corresponding high gauss levels required for testing A1360 $V_{CLP(HIGH)}$ make production testing impractical).

[4] Noise is dependent on the sensitivity of the device and the filter capacitance. An 8 mV peak-to-peak noise floor exists that is independent of device sensitivity. This noise floor attenuates proportionate to the filter capacitance (and device bandwidth).

[5] Unit of measure (phase degrees) in reference to the magnetic input signal.

[6] High-to-low transition of output voltage is a function of external load components and device sensitivity.

[7] Raw device characteristic values before any programming.

[8] $V_{OUT(Q)UNIinit}$ typically starts below the lower clamp voltage, $V_{CLP(LOW)}$. When programming the fine quiescent duty cycle for this parameter, several codes may need to be addressed before $V_{OUT(Q)UNI}$ can be measured above $V_{CLP(LOW)}$.

[9] Bits for selecting between $V_{OUT(Q)UNI}$ and $V_{OUT(Q)BI}$ programming ranges.

[10] $V_{OUT(Q)}$ guaranteed by design.

[11] $V_{OUT(Q)}$(max) is the value available with all programming fuses blown (maximum programming code set). The $V_{OUT(Q)}$ range is the total range from $V_{OUT(Q)init}$ up to and including $V_{OUT(Q)}$(max). See Characteristic Definitions section. Quiescent Voltage Output may drift by an additional ±10 mV over the lifetime of this product.

[12] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.

[13] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.

[14] Overall programming value accuracy. See Characteristic Definitions section.

[15] Sens guaranteed by design.

[16] Sens(max) is the value available with all programming fuses blown (maximum programming code set). Sens range is the total range from $Sens_{init}$ up to and including Sens(max). See Characteristic Definitions section. Sensitivity may drift by an additional ±2% over the lifetime of this product.

[17] Programmed at 150°C and calculated relative to 25°C.

[18] Linearity is only guaranteed for output voltage ranges of ±2 V from the quiescent output for bidirectional devices and +2 V from the quiescent output for unidirectional devices. These linearity ranges are only valid within the operating output range of the device. The operating output range is confined to the region between the output clamps. Linearity may shift by up to +/- 1 % over the lifetime of this product.

[19] Symmetry error is only valid for bidirectional devices. Symmetry may shift by up to ±1% over the lifetime of this product.

[20] Percent change from actual value at V_{CC} = 5 V, for a given temperature, over the guaranteed supply voltage operating range.

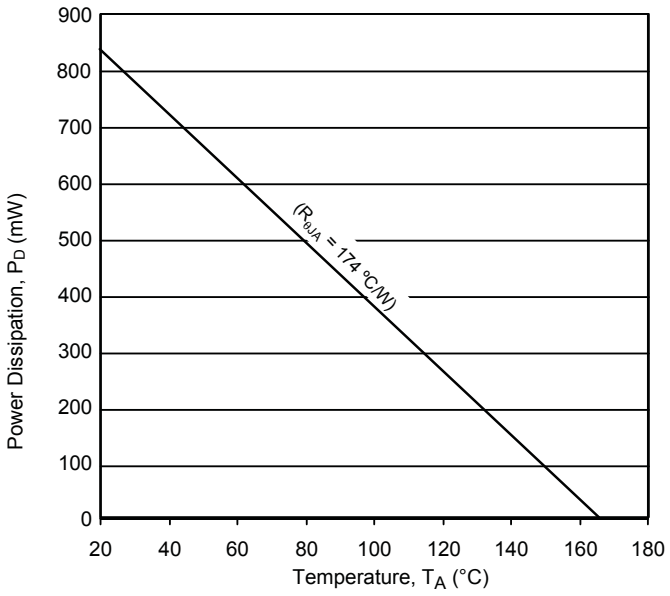
[21] Percent change from actual value at V_{CC} = 5 V, T_A = 25°C, over the guaranteed supply voltage operating range.

Thermal Characteristics may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	174	°C/W

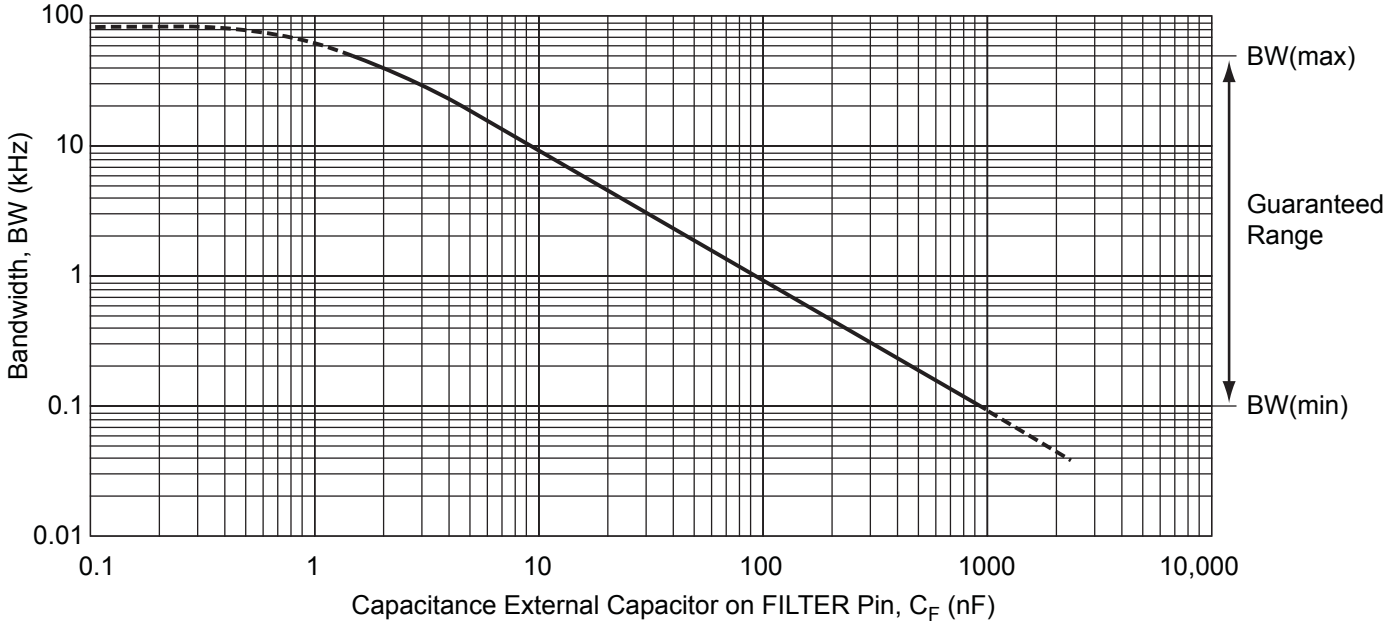
*Additional thermal information available on Allegro website.

Power Dissipation versus Ambient Temperature



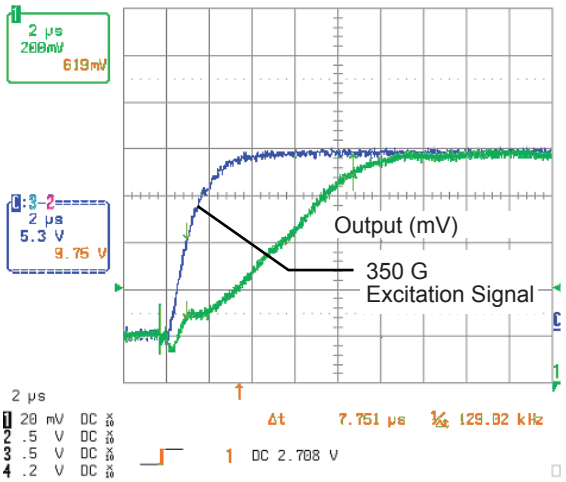
Characteristic Data

Bandwidth Range



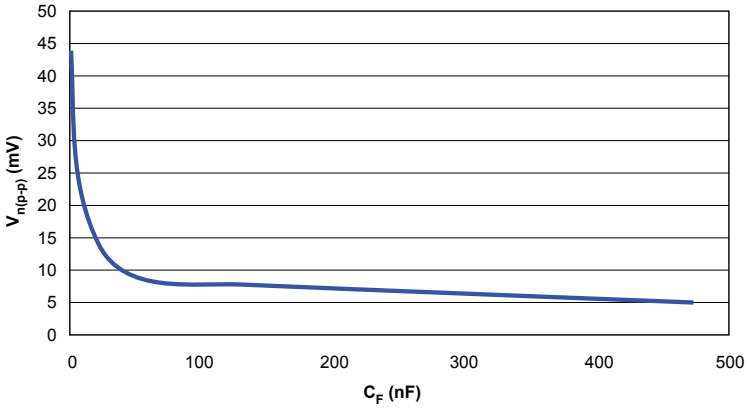
Step Response

Sens = 2.2 mV/G



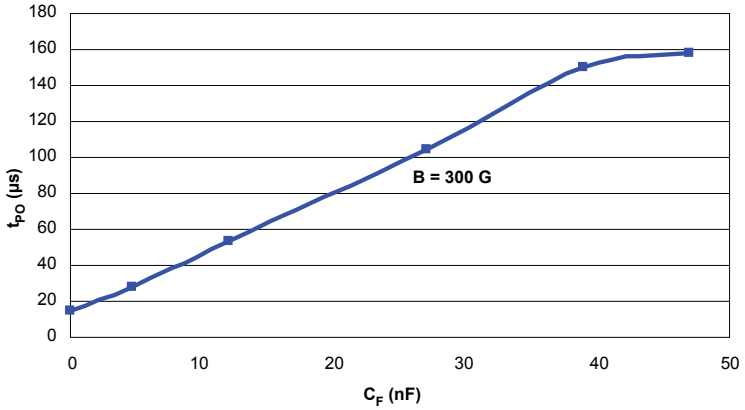
Noise versus Filter Capacitance

Sens = 6.6 mV/G



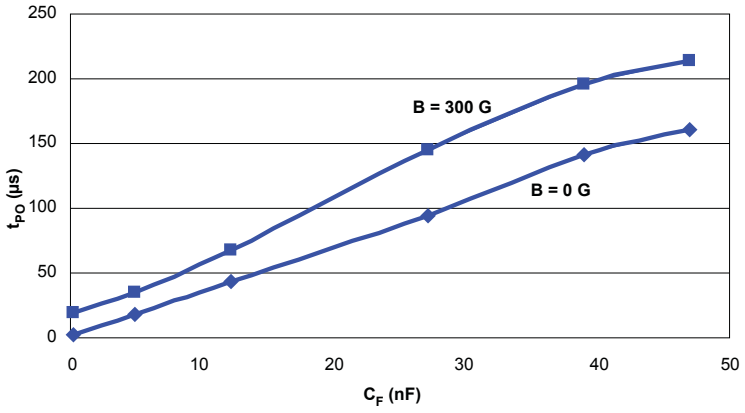
Power On Time versus Filter Capacitance

Unidirectional Device



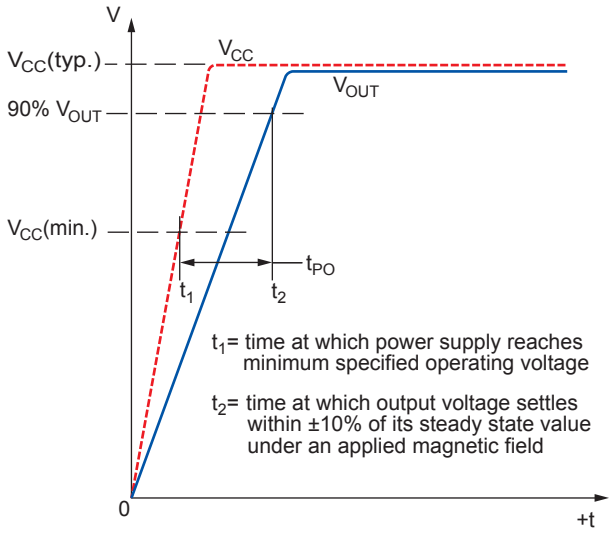
Power On Time versus Filter Capacitance

Bidirectional Device

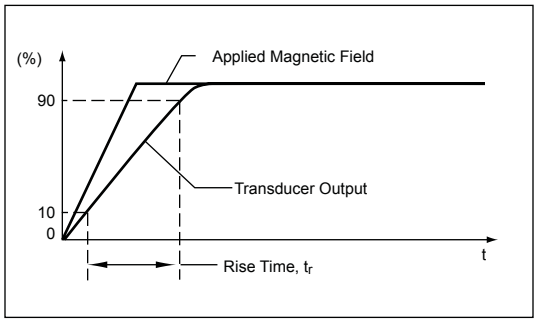


Characteristic Definitions

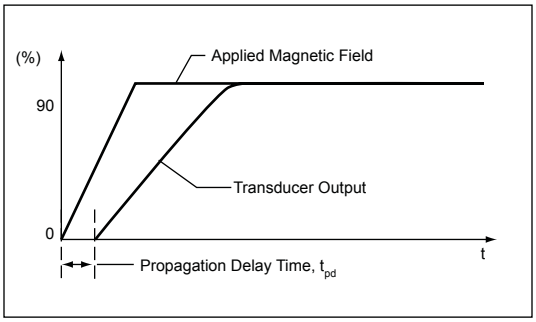
Power-On Time When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO}, is defined as: the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the following chart.



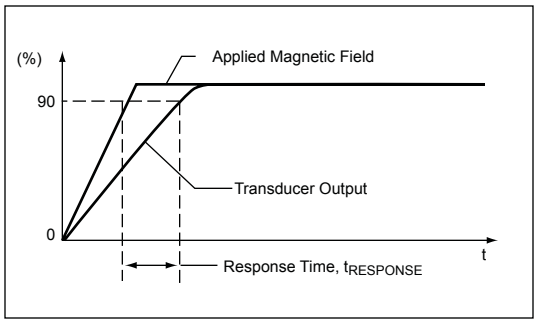
Rise Time (t_r) The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the linear device, in which $f(-3\text{ dB}) = 0.35/t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



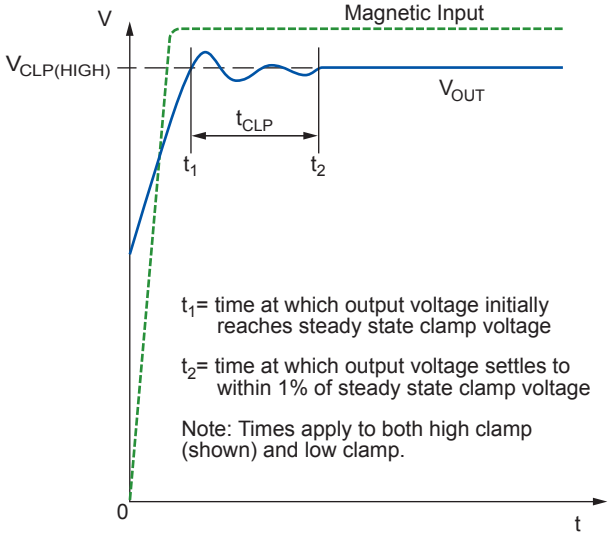
Propagation Delay Time (t_{pd}) The time required for the device output to reflect a change in the applied magnetic field. Propagation delay can be considered as a fixed time offset and may be compensated.



Response Time ($t_{RESPONSE}$) The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the device reaches 90% of its output corresponding to the applied magnetic field.

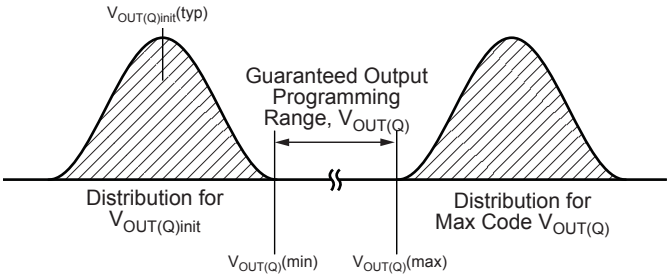


Delay to Clamp A large magnetic input step may cause the clamp to overshoot its steady state value. The Delay to Clamp, t_{CLP}, is defined as: the time it takes for the output voltage to settle within ±1% of its steady state value, after initially passing through its steady state voltage, as shown in the following chart.



Quiescent Voltage Output In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, has a constant ratio to the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Guaranteed Quiescent Voltage Output Range The quiescent voltage output, $V_{OUT(Q)}$, can be programmed around its nominal value of 2.5 V, within the guaranteed quiescent voltage range limits: $V_{OUT(Q)}$(min) and $V_{OUT(Q)}$(max). The available guaranteed programming range for $V_{OUT(Q)}$ falls within the distributions of the initial, $V_{OUT(Q)init}$, and the maximum programming code for setting $V_{OUT(Q)}$, as shown in the following diagram.



Average Quiescent Voltage Output Step Size The average quiescent voltage output step size for a single device is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)init}}{2^n - 1} . \quad (1)$$

where:

n is the number of available programming bits in the trim range,

$2^n - 1$ is the value of the maximum programming code in the range, and

$V_{OUT(Q)maxcode}$ is the quiescent voltage output at code $2^n - 1$.

Quiescent Voltage Output Programming Resolution The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) . \quad (2)$$

Quiescent Voltage Output Drift Through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent voltage output, $V_{OUT(Q)}$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} . \quad (3)$$

$V_{OUT(Q)}$, should be calculated using the actual measured values of $V_{OUT(Q)(TA)}$ and $V_{OUT(Q)(25°C)}$, rather than programming target values.

Sensitivity The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined for bipolar devices as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG} , \quad (4)$$

and for unipolar devices as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(Q)}}{BPOS} , \quad (5)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range The magnetic sensitivity, Sens, can be programmed around its nominal value, 0.7 to 16 mV/G depending on device type, within the sensitivity range limits: Sens(min) and Sens(max). Refer to the Guaranteed Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Sensitivity Step Size Refer to the Average Quiescent Voltage Output Step Size section for a conceptual explanation.

Sensitivity Programming Resolution Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{\text{Sens}} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right) \quad , \qquad (6)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The ideal value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{\text{EXPECTED(TA)}} = Sens_{T1}\,[1 + TC_{\text{SENS}}\,(T_A - T1) / 100\%] \qquad (7)$$

$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ and TC_{SENS} rather than programming target values.

Sensitivity Drift Due to Package Hysteresis Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling.

For purposes of specification, the sensitivity drift due to package hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{\text{PKG}} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \qquad (8)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The 136x family is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$\begin{aligned} Lin_{\text{ERRPOS}} &= \left(1 - \frac{Sens_{\text{BPOS2}}}{Sens_{\text{BPOS1}}}\right) \times 100\% \quad , \\ Lin_{\text{ERRNEG}} &= \left(1 - \frac{Sens_{\text{BNEG2}}}{Sens_{\text{BNEG1}}}\right) \times 100\% \quad , \end{aligned} \qquad (9)$$

where:

$$Sens_{Bx} = \frac{|V_{\text{OUT(B}x\text{)}} - V_{\text{OUT(Q)}}|}{B_x} \quad , \qquad (10)$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent voltage output such that $|B_{POS2}| = 2 \times |B_{POS1}|$ and $|B_{NEG2}| = 2 \times |B_{NEG1}|$. Then:

$$Lin_{\text{ERR}} = \max(Lin_{\text{ERRPOS}}, Lin_{\text{ERRNEG}}) \quad . \qquad (11)$$

Note that unipolar devices only have positive linearity error, Lin_{ERRPOS}.

Symmetry Sensitivity Error The magnetic sensitivity of an A136x device is constant for any two applied magnetic fields of equal magnitude and opposite polarities.

Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \qquad (12)$$

where $Sens_{Bx}$ is as defined in equation 4, and B_{POS} and B_{NEG} are positive and negative magnetic fields such that $|B_{POS}| = |B_{NEG}|$. Note that the symmetry error specification is only valid for bipolar devices.

Ratiometry Error The A136x devices feature ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltage, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, are proportional to the supply voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (13)$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSENS}$ (%), for a given supply voltage, V_{CC}, is defined as:

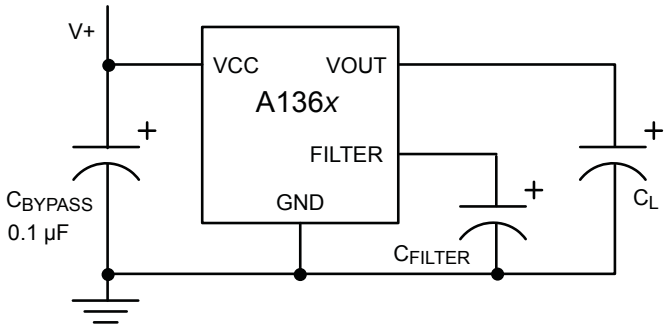
$$Rat_{ERRSENS} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (14)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad , \qquad (15)$$

where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Typical Application Drawing



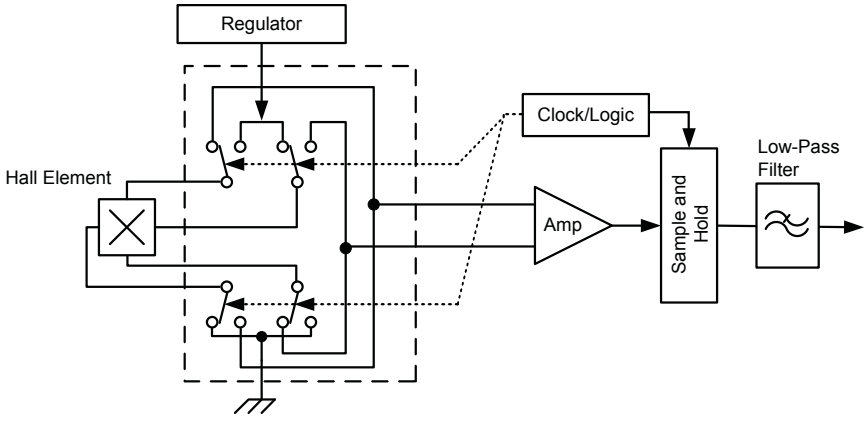
Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall device. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process.

The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the dc offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated dc offset is suppressed. The chopper stabilization technique uses a 210 kHz high frequency clock.

For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (420 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

Programming Guidelines

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VOUT pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value.

There are three voltage levels that must be taken into account when programming. These levels are referred to as *high*, $V_{P(HIGH)}$, *mid*, $V_{P(MID)}$, and *low*, $V_{P(LOW)}$. There are two programming pulse levels. A *high* voltage pulse, V_{PH}, refers to a $V_{P(LOW)}$ $-V_{P(HIGH)}$ $-V_{P(LOW)}$ sequence. A *mid* voltage pulse, V_{PM}, refers to a $V_{P(LOW)}$ $-V_{P(MID)}$ $-V_{P(LOW)}$ sequence.

The 136x features four modes used during programming: Hold mode, Try mode, Blow mode, and Lock mode:

- In Hold mode, the value of two programmable parameters may be set and measured simultaneously. The parameter values are stored temporarily, and reset after cycling the supply voltage.
- In Try mode, the value of a single programmable parameter may be set and measured. The parameter value is stored temporarily, and resets after cycling the supply voltage. (Note that other parameters cannot be accessed simultaneously in this mode.)
- In Blow mode, the value of a single programmable parameter may be set permanently by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially.
- In Lock mode, a device-level fuse is blown, blocking the further programming of all parameters.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Any programmable variable power supply can be used to generate the pulse waveforms, although Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro Web site On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

Definition of Terms

Register One of several sections of the programming logic that control the bit fields storing the code choices for setting programming modes and programmable parameters.

Bit Field The set of internal fuses controlled by a single register. Each fuse in a bit field represents a binary digit in the code setting for that register. The internal logic of the device interprets that code and applies the result to a programmable parameter of the device. Individual fuses can be temporarily activated for testing of the result, or permanently blown.

Key A series of one or more consecutive mid voltage pulses that indicate by their quantity the register being addressed. The quantity of mid voltage pulses corresponds to the decimal equivalent of the binary value of the register being addressed. For example, the LSB of a zone is bit 0 (binary 0), corresponding to register 1, and indicated by key 1 (decimal 1), a single mid voltage pulse.

Code A series of one or more consecutive mid voltage pulses that indicate by their quantity the combination of fuses to be activated or blown in the currently-selected register. The quantity of pulses in the code corresponds to the decimal equivalent of the binary value of the bits (links) to be activated or blown. The LSB of a bit field is bit 0, activated by code 1 (decimal 1), a single mid voltage pulse.

Addressing Indicating the target register or bit field setting by incrementing the key or code by means of pulse trains of consecutive mid voltage pulses transmitted through the VOUT pin of the device. During the addressing process, each parameter can be measured, before either blowing the fuses to permanently set the programming code (and parameter value), or cycling the power to reset the unblown bits.

Zone The 136x programming logic is designed to accept up to two different key-code combinations sequentially without cycling the supply. The first key-code combination is interpreted as addressing a register in the first zone, and the second key-code combination is interpreted as addressing a register in the second zone. All of the parameter registers are located in either the first or second zone. The first zone must be entered and exited before the parameter registers available in the second zone may be accessed.

Fuse Blowing Applying a high voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. After a bit (fuse) has been blown, it cannot be reset.

Blow Pulse A high voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, protocol at T_A = 25°C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Units
Programming Voltage	$V_{P(LOW)}$	Measured at the VOUT pin.	–	–	5.5	V
	$V_{P(MID)}$		14	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the VOUT and GND pins during programming, to provide the current necessary for fuse blowing.	300	–	–	mA
Pulse Width	t_{LOW}	Duration of $V_{P(LOW)}$ voltage level for separating $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses, and delay time after the final V_{BLOW} pulse.	40	–	–	µs
	t_{ACTIVE}	Duration of $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses for register selection or bit field addressing.	40	–	–	µs
	t_{BLOW}	Duration of $V_{P(HIGH)}$ pulses for fuse blowing.	40	–	–	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	5	–	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ or $V_{P(MID)}$ to $V_{P(LOW)}$.	5	–	100	µs

Programming Procedures

Parameter Selection

Each of the four programmable parameters can be accessed through its corresponding parameter register. These registers are located in two distinct zones in the A136x devices:

Zone 1, Register 1:
• Fine sensitivity, Sens
Zone 2, Register 1:
• Fine quiescent voltage output, $V_{OUT(Q)}$
Zone 2, Register 2:
• Coarse quiescent voltage output, $V_{OUT(Q)}$
• Overall device locking, LOCK

To select the register in the first zone, a sequence of one V_{PH} pulse, the key for the register, and a second V_{PH} pulse (with no VCC supply interruptions) must be applied serially to the VOUT pin. The pulse train used for selection of the first register, key 1, is shown in figure 1.

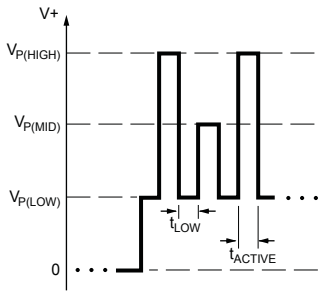


Figure 1. Voltage pulse sequence required to select the first programmable register in the first zone.

After the falling edge of the second V_{PH} pulse, the bit field of the selected register may be addressed with the appropriate code (see Bit Field Addressing section, below).

The first zone must be traversed before the second zone can be accessed. After completing any bit field addressing in the first zone, to enter the second zone, apply a third V_{PH} pulse. As in the first zone, this must be followed by the key for the parameter register, then a V_{PH} pulse and the bit field code (with no VCC supply interruptions).

Bit Field Addressing

After the register of a programmable parameter has been selected as described above, the code pulses must be applied serially to the VOUT pin with no VCC supply interruptions. As each additional pulse in the code is transmitted, the overall setting of the bit field increments by 1, up to the maximum possible code for that register (see the Programming Logic table). The A136x logic interprets the overall setting (the binary sum of all of the activated or blown fuses) and applies it to the value of the parameter, according to the step size for the parameter (shown in the Electrical Characteristics table).

Addressing activates the corresponding fuse locations in the given bit field by incrementing the binary value of an internal DAC. Measurements can be taken after each pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

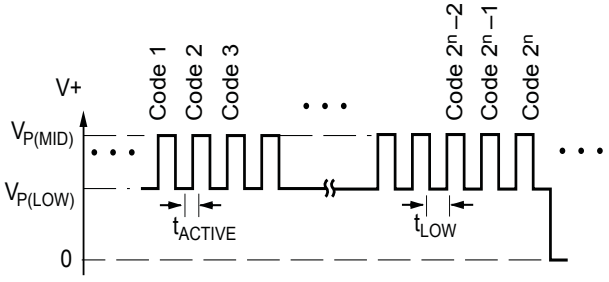


Figure 2. Bit field addressing pulse train. Addressing the bit field by incrementing the code causes the programmable parameter value to change. The number of bits available for a given programming code, n, varies among parameters; for example, the bit field for Sensitivity has 8 bits available, which allows 255 separate codes to be used.

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a high voltage pulse, called a blow pulse, of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. To accomplish this, the code representing the desired parameter value must be translated to a binary number. For example, as shown in figure 3, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed and blown. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2, is acceptable.

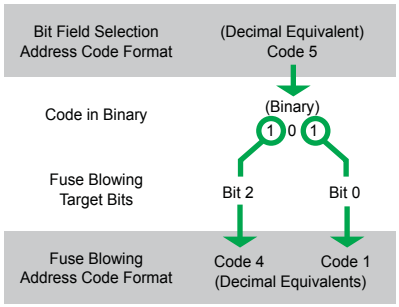


Figure 3. Example of code 5 broken into its binary components, equaling code 4 and code 1.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

Locking the Device

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters. See the Lock Mode section for lock pulse sequence.

Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VOUT pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The C_{BLOW} blowing capacitor must be replaced in the final application with a suitable C_L. (The maximum load capacitance is 10 nF for proper operation.) The power supply used for programming must be capable of delivering at least 26 V and 300 mA. Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming order is recommended:
  1. Coarse $V_{OUT(Q)}$
  2. Sens
  3. $V_{OUT(Q)}$
  4. LOCK (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

Programming Modes

Hold Mode

Hold mode allows multiple programmable parameters to be tested simultaneously without permanently setting any values. With the 136x programming logic, only two parameters located in different zones can be addressed together. For example, only the sensitivity and fine quiescent voltage offset parameters can be temporarily set and tested simultaneously without permanently setting their values. For unidirectional devices, the unidirectional bit must be permanently blown before using the Hold Mode to temporarily set and test the sensitivity and fine quiescent voltage offset.

Powering the VCC supply automatically causes the device to enter the first zone. Applying a high pulse, mid pulse, high pulse sequence selects the Sensitivity register. The sensitivity can be set to the desired value by applying the appropriate code pulses.

The next high-level pulse transitions the programming logic into the second zone. Applying one mid level pulse causes the logic to enter the Fine Quiescent Voltage Output register, and another high-level pulse causes the logic to enter the Fine Quiescent Voltage Output bit field. The fine quiescent voltage output can be set to the desired level by applying the appropriate number of mid-level pulses to the VOUT pin. (See figure 4.)

The addressed parameter values will be stored in the device logic even after the programming drive voltage is removed from the VOUT pin, allowing the output to be measured at any time during the programming process.

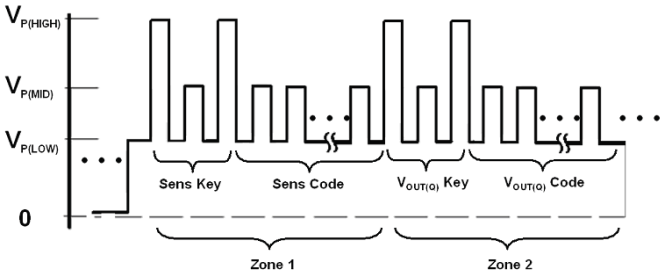


Figure 4. Hold sequence for testing Sens and $V_{OUT(Q)}$ parameters together.

After addressing and measuring the device output, cycle the supply to reset all of the register values. Registers can be addressed and re-addressed an indefinite number of times. Once the final desired code is found for each register, cycle the supply and blow the bit field using Blow mode.

Note: For accurate time measurements, the blow capacitor, C_{BLOW}, should be removed during output voltage measurement. Also note that both the Sensitivity and Fine Quiescent Voltage Output registers should not be blown simultaneously. See the Blow Mode section for additional information.

Try Mode

Try mode allows a single programmable parameter to be tested without permanently setting its value. Try mode is a required step of parameter blowing. (See the Blow Mode section for additional information.) To select a parameter register in the first zone, power the supply and enter the appropriate key-code pulse combination (see figure 5). To select a parameter register in the second zone, power the supply and apply two high voltage pulses, followed by the appropriate key-code pulse combination (see Figure 6). When addressing the bit field, each V_{PM} pulse increments the value of the parameter register, up to the maximum possible code (see the Programming Logic table). The addressed parameter value is stored in the device even after the programming drive voltage is removed from the VOUT pin, allowing its value to be measured.

Note: For accurate time measurements, the blow capacitor, C_{BLOW}, should be removed during output voltage measurement. To reset the bit field, and thus the value of the programmable parameter, cycle the VCC supply voltage.

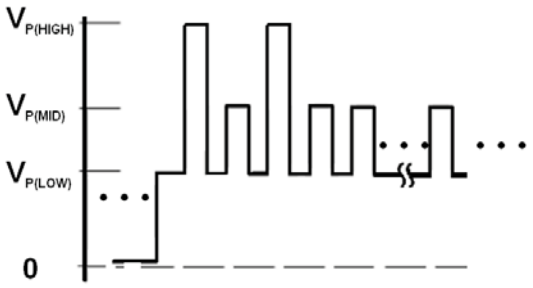


Figure 5. Pulses to enter Try mode, zone 1. Example shown is for addressing the Sensitivity register. After addressing desired code, cycle the supply to reset the bit field or apply a blow pulse to make the parameter value permanent.

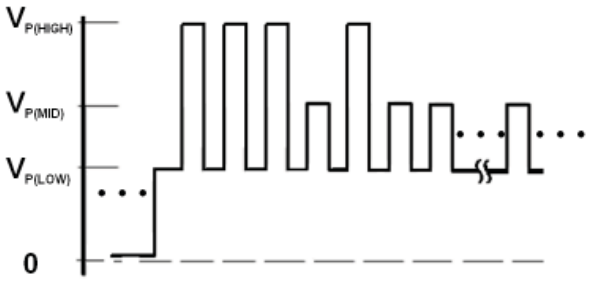


Figure 6. Pulses to enter Try mode, zone 2. Example shown is for addressing the Fine Quiescent Voltage Output register. After addressing desired code, cycle the supply to reset the bit field or apply a blow pulse to make the parameter value permanent.

Blow Mode

After the required value of the programmable parameter is addressed using Try mode, its corresponding code can be blown to make its value permanent. To do this, select the required parameter register and the appropriate code. (See the Fuse Blowing section. Recall that each bit of a desired code must be blown individually before cycling the supply.) If the desired parameter is in the first zone, enter the appropriate key-code combination and then apply two high-level voltage pulses followed by an additional blow pulse. If the desired parameter is in the second zone, enter the appropriate key-code combination and then apply a single blow pulse on the VOUT pin. This is diagrammed as follows:

Zone 1: $V_{PH} \rightarrow$ Key $\rightarrow V_{PH} \rightarrow$ Code for Single Bit $\rightarrow V_{PH} \rightarrow V_{PH} \rightarrow V_{PH}$

Zone 2: $V_{PH} \rightarrow V_{PH} \rightarrow V_{PH} \rightarrow$ Key $\rightarrow V_{PH} \rightarrow$ Code for Single Bit $\rightarrow V_{PH}$

Note: During a single blowing sequence, only one programmable parameter in a single zone should be set at a time. After each blow sequence the supply should be cycled before attempting to blow additional bits.

Lock Mode

To lock the device, address the LOCK bit and apply a blow pulse with C_{BLOW} in place. The LOCK bit is located in zone 2, register 2, code 4. After locking the device, no future programming of any parameter is possible.

The lock sequence is:

$V_{PH} \rightarrow V_{PH} \rightarrow V_{PH} \rightarrow V_{PM} \rightarrow V_{PM} \rightarrow V_{PH} \rightarrow V_{PM} \rightarrow V_{PM} \rightarrow V_{PM} \rightarrow V_{PM} \rightarrow V_{PM} \rightarrow V_{PH}$

Programming State Machine

Initial State

After system power-up, the programming logic is reset to a known state. This is referred to as the *Initial* state. All the bit field locations that have intact fuses are set to logic 0. While in the Initial state, any V_{PM} pulses on the VOUT pin are ignored. To enter the zone 1 Parameter Selection state, apply a single V_{PH} pulse on VOUT pin. To enter the zone 2 Parameter Selection state, apply a sequence of three V_{PH} pulses on the VOUT pin.

Parameter Selection State

This state allows the selection of the parameter register containing the bit fields to be programmed. To select a parameter register within the chosen zone, increment through the keys by sending V_{PM} pulses on the VOUT pin. Register keys select among the following programming parameters in zone 1:

1 pulse – Sens,

and the following programming parameters in zone 2:

1 pulse – $V_{OUT(Q)}$

2 pulses – Coarse $V_{OUT(Q)}$ and LOCK

To enter the Bit Field Addressing state, send one V_{PH} pulse on the VOUT pin.

Note: When parameter selection for zone 1 is bypassed (by sending a second V_{PH} pulse) no register is selected, and V_{PM} pulses are ignored until after the V_{PH} pulse is sent to enter zone 2.

Bit Field Addressing State

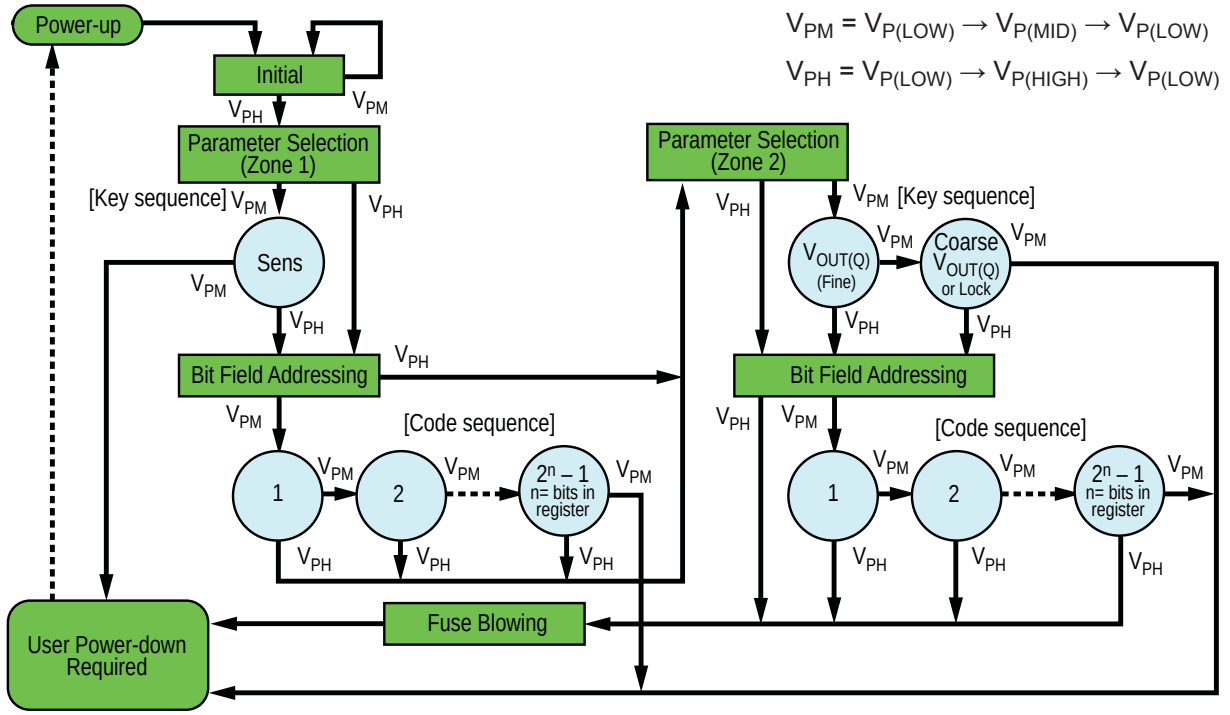
This state allows the selection of the individual bit fields to be programmed in the selected parameter register (see the Programming Logic table). To leave this state, either cycle device power or blow the fuses for the selected code.

Note: Merely addressing the bit field does not permanently set the value of the selected programming parameter; fuses must be blown to do so.

Fuse Blowing State

To blow an addressed bit field, apply a V_{PH} pulse on the VOUT pin. Power to the device should then be cycled before additional programming is attempted.

Note: Each bit representing a decimal code must be blown individually (see the Fuse Blowing section).



Programming Logic Table

Programmable Parameter		Bit Field Address		Description
Zone	Register Selection (Key)	Binary Format (MSB → LSB)	Decimal Equivalent Code	
1	Sens (1)	00000000	0	Initial value ($Sens_{init}$)
		11111111	255	Maximum value of sensitivity (Sens) in range
2	$V_{OUT(Q)}$ (1)	00000000	0	Initial value for selected programming region ($V_{OUT(Q)init}$)
		11111111	255	Maximum value of fine $V_{OUT(Q)}$ in range for selected bidirectional or unidirectional device
	Coarse $V_{OUT(Q)}$ (2)	00000001	1	Switch from default bidirectional ($V_{OUT(Q)BI}$) device to ($V_{OUT(Q)UNI}$) device
	LOCK (2)	00000100	4	LOCK bit, enables permanent locking of all programming bit fields in the device

Constructing a Current Sensor Using the A136x

To construct a current sensor using the A136x, first consider a current carrying wire that we want to observe. As dictated by Ampere's Law, a magnetic field is produced around the wire that is proportional to the amount of current flowing through the wire. By passing this wire through a soft magnetic core, the magnetic flux produced by the wire can be concentrated and directed through a gap in the core. The magnetic flux density can be measured by inserting the A136x SIP into the gap in the core. As a result, the output of the A136x device will be proportional to the amount of current flowing through the wire.

The example feedthrough current sensing setup shown below (figure 7) has a core made of "mu metal" that is 2 mm thick and 4 mm wide. The inner radius of the core is 14.5 mm and the outer radius is 18.5 mm. The wire going through the center of the core has a radius of 9 mm. Using this setup with a gap of 1.7 mm, a field strength results that is on the order of 7 G/A at the Hall element in the A136x.

The recommended core material for construction of the concentrator depends on the specific application. If high flux saturation is desired, then an alloy such as HyPerm49 is recommended. For lower-current level sensing applications, a material such as HyMu80 may be desired. (HyMu80 has lower magnetic flux saturation than HyPerm49, therefore more HyMu80 material is required to carry the same amount of flux compared to Hyperm49.) If frequency response is a concern, then eddy currents can be reduced by either laminating the HyPerm49 or HyMu80 alloys, or by using a ferrite core.

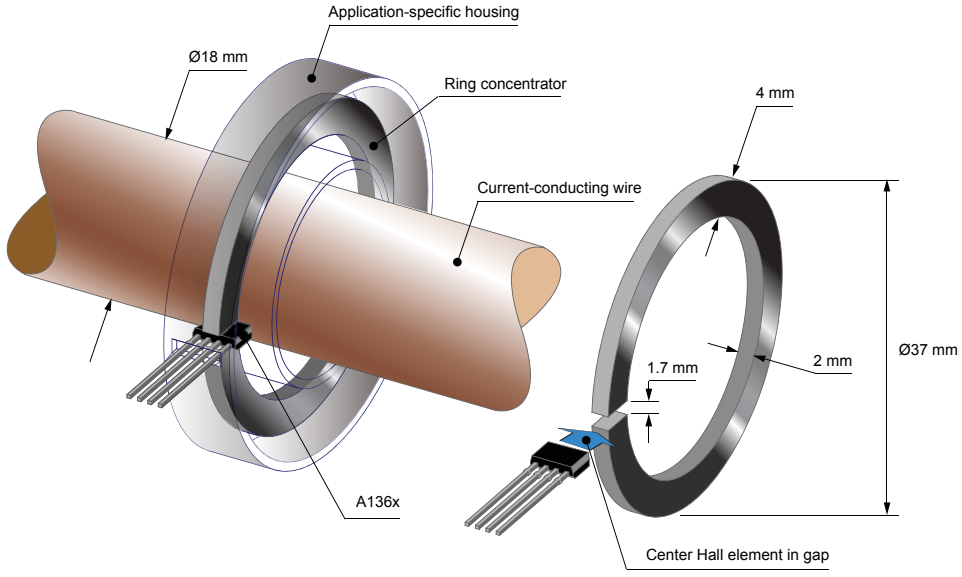


Figure 7. The example current sensor setup used to generate the data in this section was constructed with a split-ring concentrator and an A136x device. A copper wire was fed through the concentrator, and the A136x placed in its gap. This approximates a typical ammeter application on a thick wire, such as shown in the left view. Note that such applications usually have a protective housing, which should be taken into consideration when designing the final application. The housing is beyond the scope of this example.

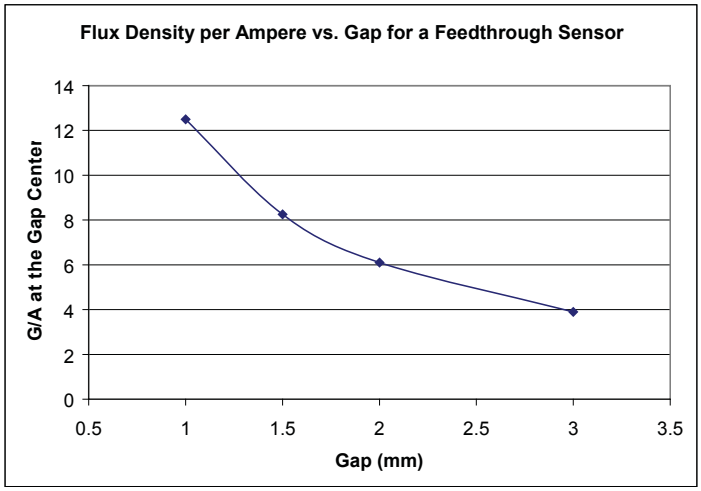


Figure 8. The flux density per ampere measured by the A136x Hall sensor IC is related to the core gap, as shown. This figure assumes that the current sensing application is constructed using the example setup.

The flux density measured by the A136x SIP is related to the size of the gap cut into the core. The larger the gap in the core, the smaller the flux density per ampere of applied current (see figure 8).

Figure 9 depicts the magnetic flux density through the center of the SIP as a function of SIP to core alignment. Note that a core with a larger cross-sectional area would reduce the attenuation in flux density that results from any SIP misalignment. The flat portion of the curve in figure 9 would span a larger distance in millimeters if the cross-sectional area of the core were increased.

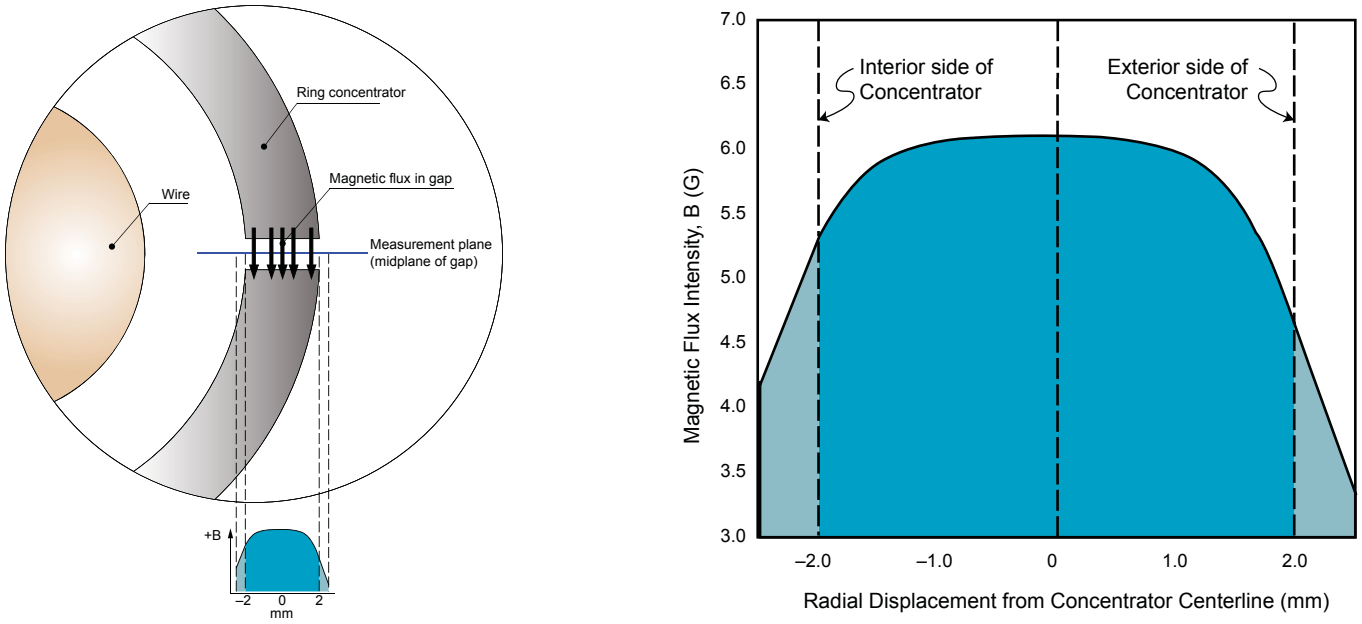


Figure 9. Side view of example current-conducting wire and split ring concentrator (left), and magnetic profile (right) through the midplane of the gap in the split ring concentrator. The flux denisty through the center of the gap varies between the inside and the outside of the gap.

Improving Sensing System Accuracy Using the FILTER Pin

In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the sensor IC. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation, ΔV_{ATT}, is a result of the resistive divider effect between the resistance of the external filter, R_{EXT} (see figure 10), and the input impedance and resistance of the customer interface circuit, R_{INTFC}. The transfer function of this resistive divider is given by:

$$\Delta V_{ATT} = V_{OUT}\left(\frac{R_{INTFC}}{R_{EXT} + R_{INTFC}}\right) . \qquad (16)$$

Even if R_{EXT} and R_{INTFC} are designed to match, the two individual resistance values will most likely drift by different amounts over temperature. Therefore, signal attenuation will vary as a function of temperature. Note that the input impedance, R_{INTFC}, of commonly available analog-to-digital converters (ADC) can be as low as 10 kΩ.

The A136*x* contains an internal resistor with buffer amplifier that can be connected via the FILTER pin to the PCB. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor, C_{FILTER} (see figure 11) from the FILTER pin to ground. The buffer amplifier inside of the A136*x* (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in equation 16. Therefore, the A136*x* device is ideal for use in high-accuracy applications that require a large signal-to-noise ratio and cannot afford the signal attenuation associated with the use of an external RC low-pass filter.

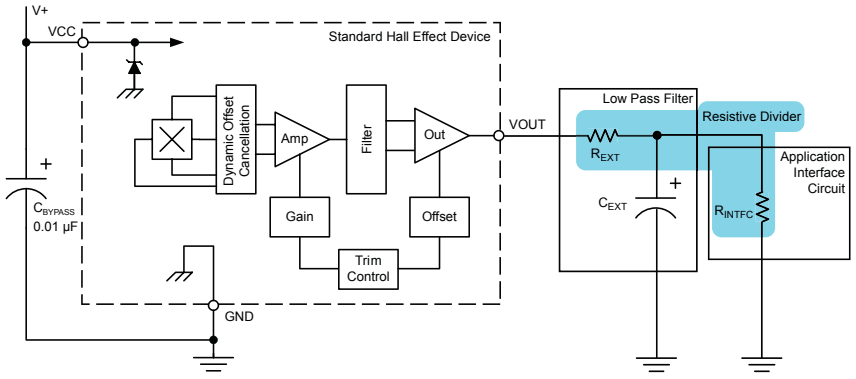


Figure 10. When a low pass filter is constructed externally to a standard Hall effect device, a resistive divider may exist between the filter resistor, $R_{EXT,}$ and the application load resistance, R_{INTFC}. This resistive divider (shaded area) will cause excessive attenuation, as given by the transfer function shown in equation 16.

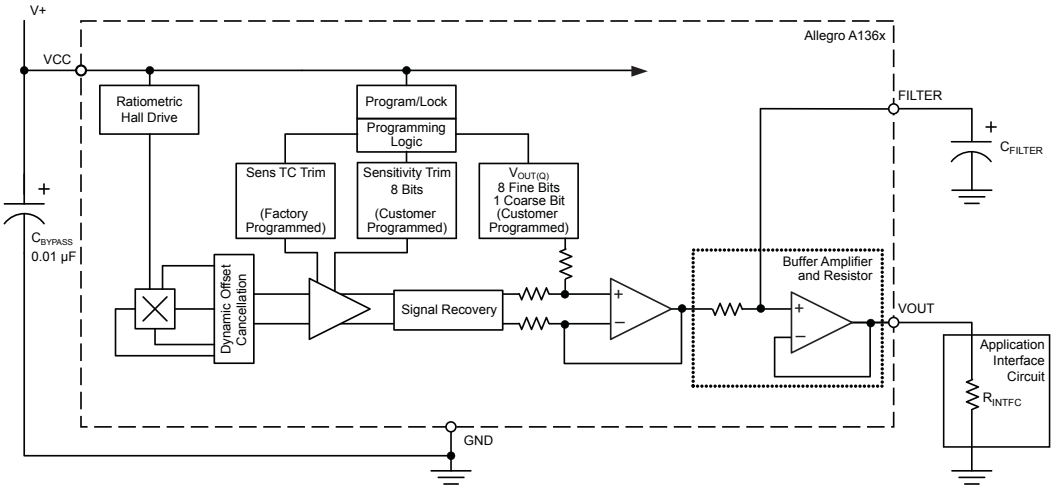
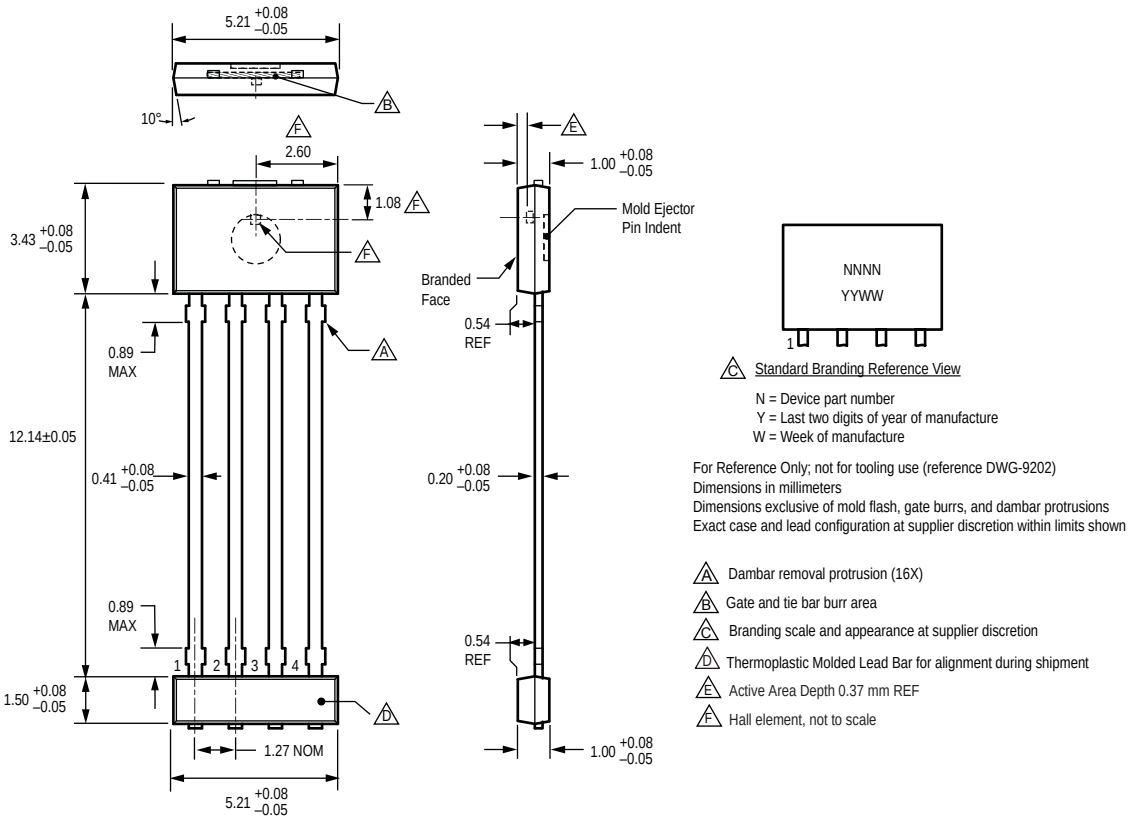


Figure 11. The FILTER pin provided on the A136x device allows separate control of SNR, avoiding the attenuation effects from the standard resistor divider solution, shown in figure 10.

Package KT, 4-Pin SIP



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